Second Year Progress Report:

Analysis and Tests for Space Qualifications of the Payloads Electronics of the NUSES Mission.

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Supervisor**: Prof Roberto Aloisio** | Co-Supervisor**: Prof Herman Lima**

16th October, 2025.

Outline

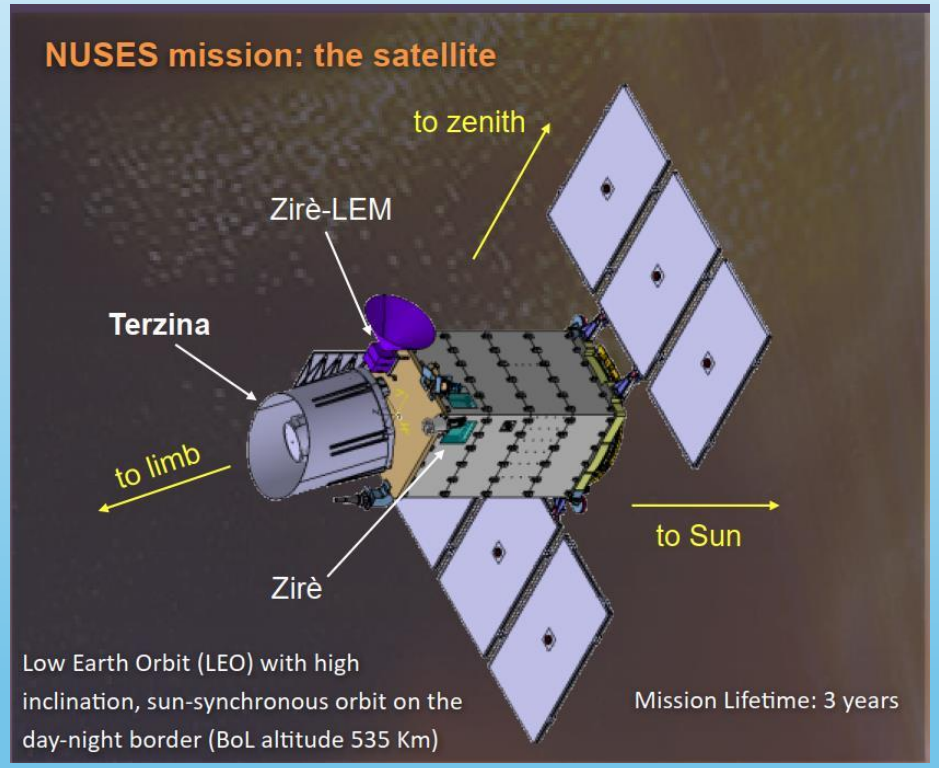
- NUSES Mission; Why FPGA reliability matters
- SEUs in FPGAs
- Mitigation: TMR + XilSEM
- Device under Test: Versal VE2302
- Test plan and use cases
- Pre-Beam: Lockstep and fault injection results
- Beam Campaing Parameters
- Next step: Terzina EQM at UniGE

Activities taken during the second year

- Completed a six-month internship in the Radiation Team at Thales Alenia Space, Rome (April 2025 – September 2025).
- Began a six-month abroad mission with the Terzina group at the University of Geneva (UniGe) from October 2025 to March 2026.
- Attended NUSES Collaboration Meeting 2024 (December 16th to 18th).
- Attended the Mentor-Siemens training on System-in-Package (SiP) technology (Innovator 3D IC) from February 26–27, 2025.

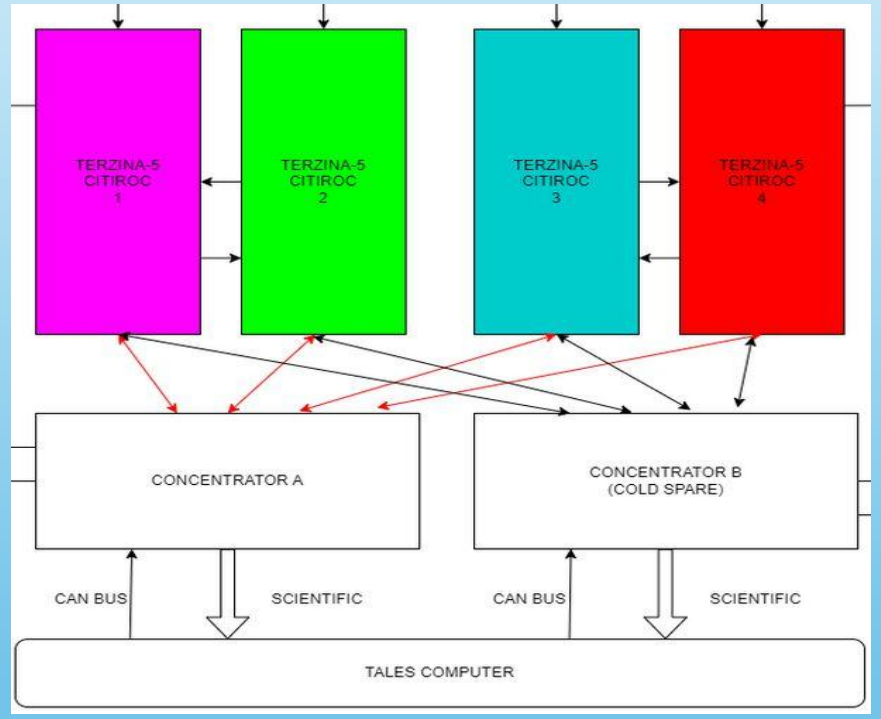
Introduction to NUSES mission

- **Mission objective:** To test new space-based detectors for astroparticle physics.
- **Payloads;**
  - **Zire;** features and scientific goals
    - Studies gamma-ray bursts and measures cosmic rays.
  - **Terzina;**
    - Targets ultra-high-energy events (neutrinos and cosmic rays >1 PeV) via EAS Cherenkov emission.
  - **Mission profile:** Sun-synchronous LEO ~550 km; ~3-year lifetime.



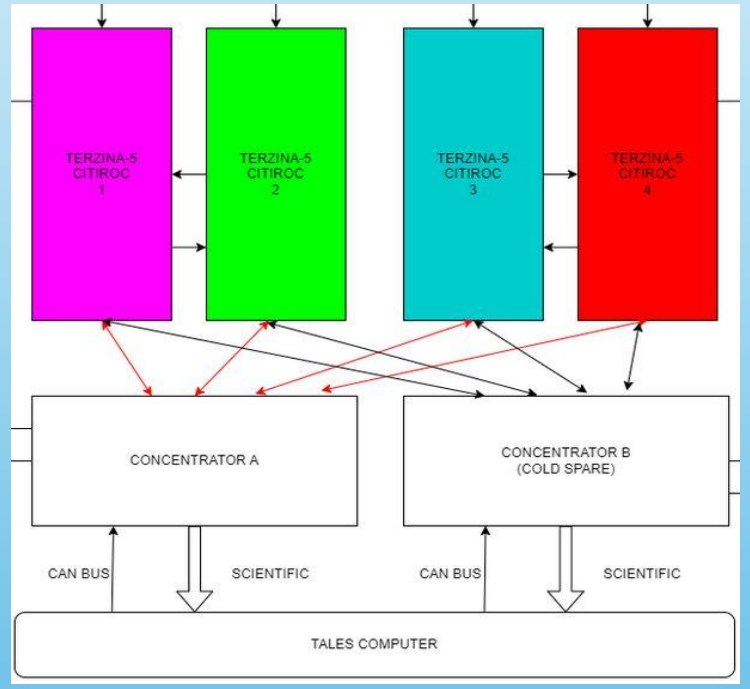
Terzina DAQ

- Designer: **Nuclear Instruments**
- DAQ system composed by;
  - DAQ boards (ADC+FPGA)
  - Data Concentrator (DC) boards
  - TAS-I computer
- Data Concentrator;
  - Uses a SoC FPGA as the central processor, with a Quad-Core ARM-64 processor.
  - Provides Scientific and Slow Control interfaces to the DAQ boards.



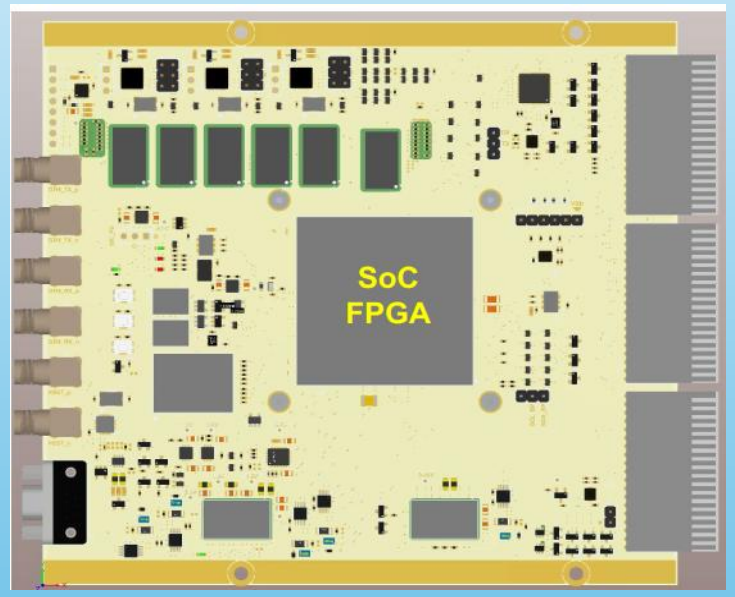
SoC FPGA: A single chip that combines hard processor cores (e.g., Arm) with FPGA fabric, so that you run software on the CPU and implement custom hardware in the fabric.

Data Concentrator



In the NUSES satellite; Terzina and Zire payloads use about 15 FPGAs (DAQ and Data Concentrator boards).

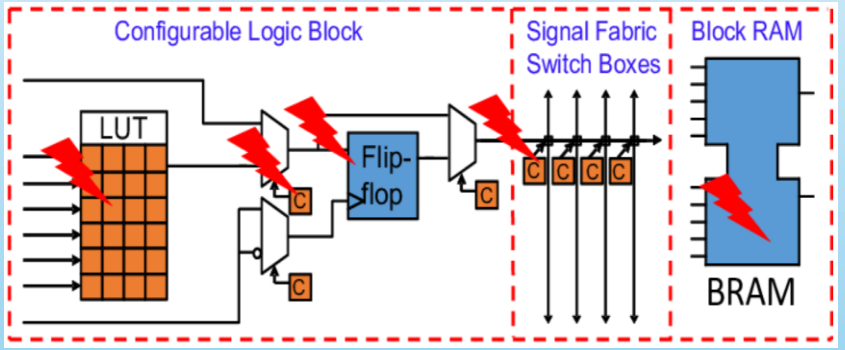
The FPGAs are critical in the operation of the DAQ: all the scientific data from the payloads flows through the FPGAs.

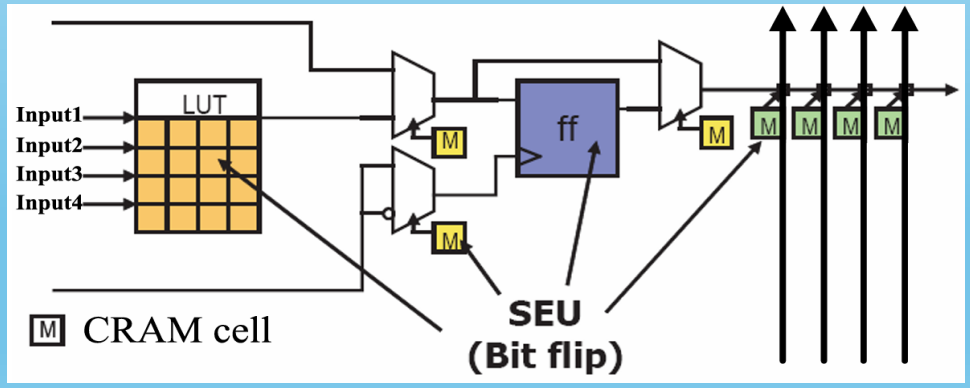


FPGA: Zynq Ultrascale+ XCZU7CG-1FFVF1517I (AMD)
Two Dual-Core Arm Cortex processors 1.3 GHz
Industrial Grade: -40ºC to +100ºC

Introduction- FPGA Vulnerability to SEU

- ✓ FPGA can be sensitive to SEUs;
  - ➢ A charged particle strike flips a bit in configuration memory (CRAM) or registers, altering logic, routing, or data.
  - ➢ Can cause temporary malfunction without permanent damage.
  - ➢ Common in space/avionics; critical for safety-critical systems.

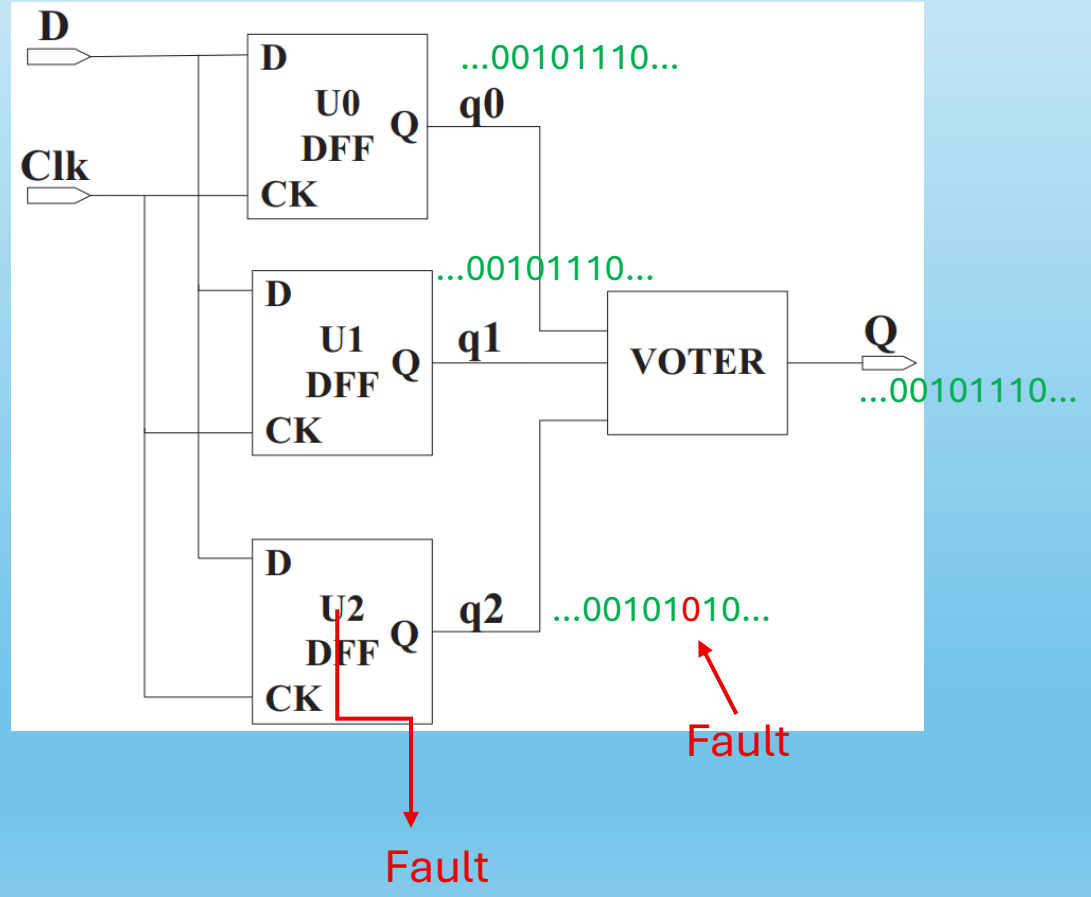




SEU (Single-Event Upset): A bit flip in sensitive nodes of electronics caused by a single ionizing particle((usually non-destructive but can cause soft errors).

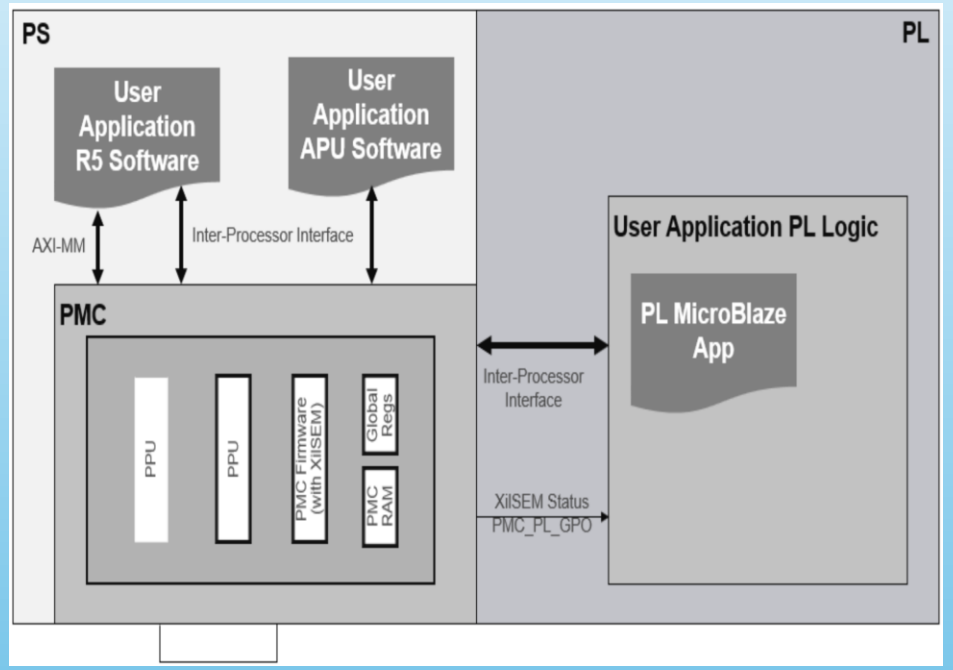
Introduction – Mitigation Techniques (TMR)

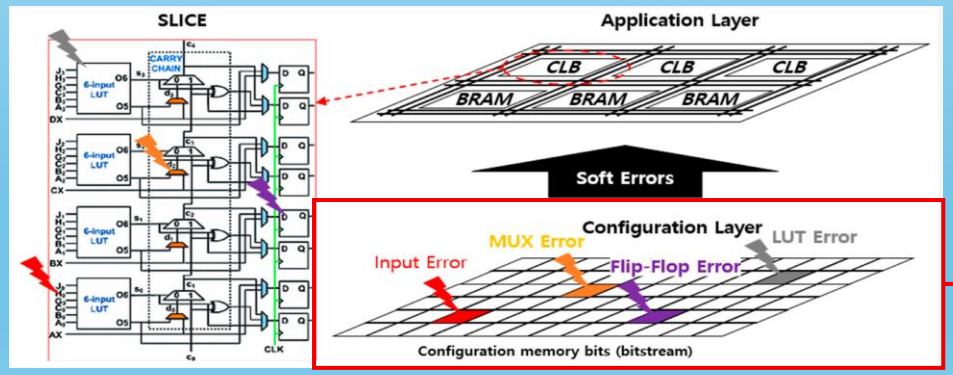
- ✓ **Triple Modular Redundancy** (TMR):
  - ➢ Three identical modules (U0, U1, U2) perform the same operation in parallel.
  - ➢ A “Voter” circuit outputs the majority result — masking errors if one module fails.
  - ➢ Protects against SEUs by ensuring correct output even if one flip-flop is corrupted.



Xilinx Soft Error Mitigation (XilSEM) library

- Updated version of the Soft Error Mitigation IP (SEM IP) used as internal soft error scrubber in the previous Xilinx FPGA generations.
- Runs on PLM (PMC). Scans CRAM and NPI Registers; detects & corrects soft errors.
- Notifies clients via IPI (APU/RPU or MicroBlaze).
- Modes: deferred start; detect/correct; event logging.



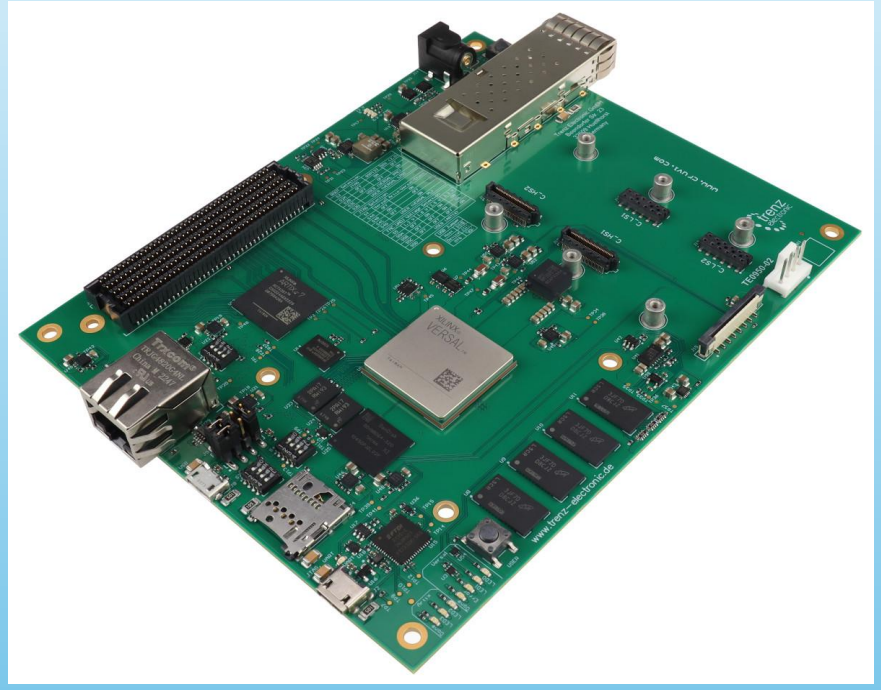


XilSEM Scrubbing

RPU = Real Time Processing Unit, Arm Cortex R5F cluster. APU = Application Processing Unit, dual Arm Cortex A72 cluster. PMC = Platform Management Controller. PLM = Platform Loader and Manager. IPI = Inter Processor Interrupt. NPI = Network on Chip Programming Interface.

Versal ACAP Reliability with XilSEM

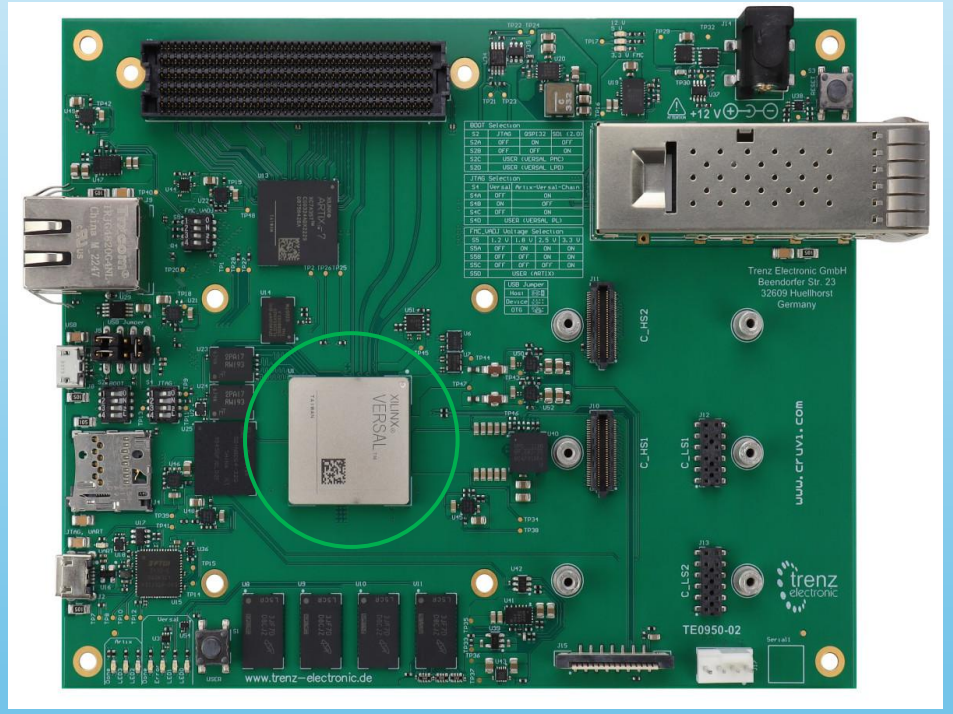
- Part of TAS WP5
- Task 5.5: Qualification of High Complexity Devices
- Purpose of WP5 : study of radiation effects induced by VHE heavy ions on a set of technologies representative of current state-of-the-art COTS electronics.
- TAS selected for the qualification of high complexity devices a new version of the VERSAL Edge FPGA SoC device family: VE2302.



Versal ACAP: Versal Adaptive Compute Acceleration Platform

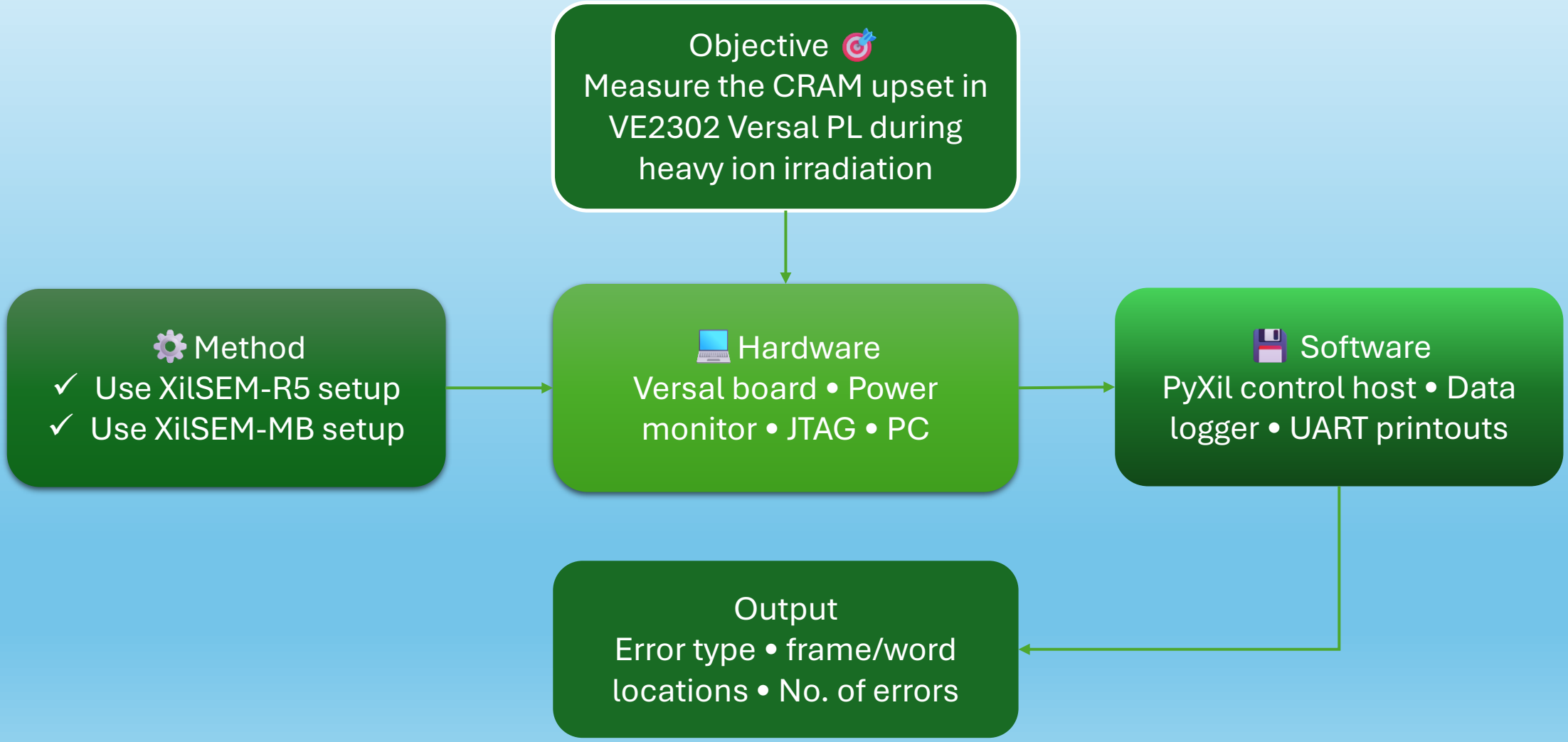
Versal Overview

- **Device feature:**
  - Heterogeneous SoC: Programmable Logic (PL), Processing System (PS), AI Engine (AIE).
  - Programmable logics: 329K System Logic Cells, 150.272 LUTs.
  - Processing System: APU Dual core ARM A72, RPU Dual Core ARM R5F, PMC MicroBlaze (Rad Hard).
  - Other Platform features: 103 Mb RAM (32 Mb Accelerator RAM).
  - Device is based on 7nm FinFET technology from TSMC foundry.



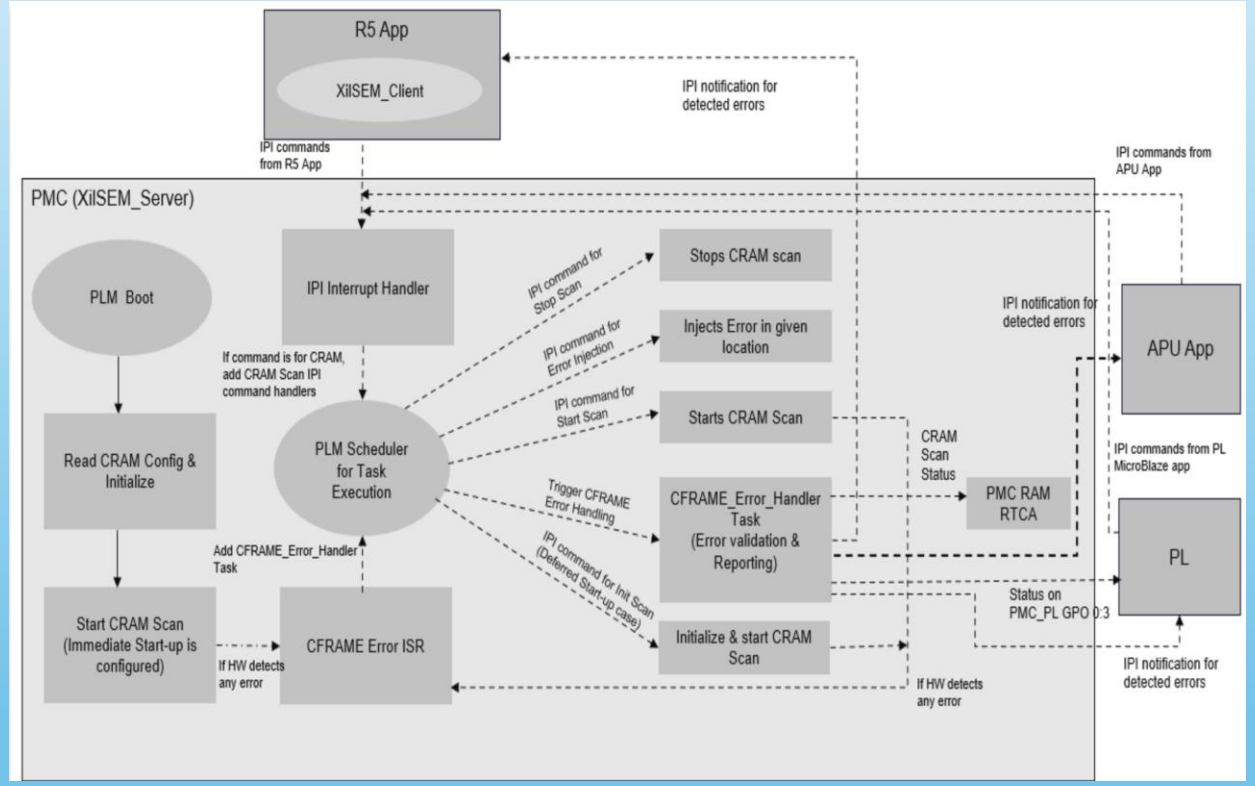
RPU = Real Time Processing Unit, Arm Cortex R5F cluster. APU = Application Processing Unit

Campaign Overview



Use Cases

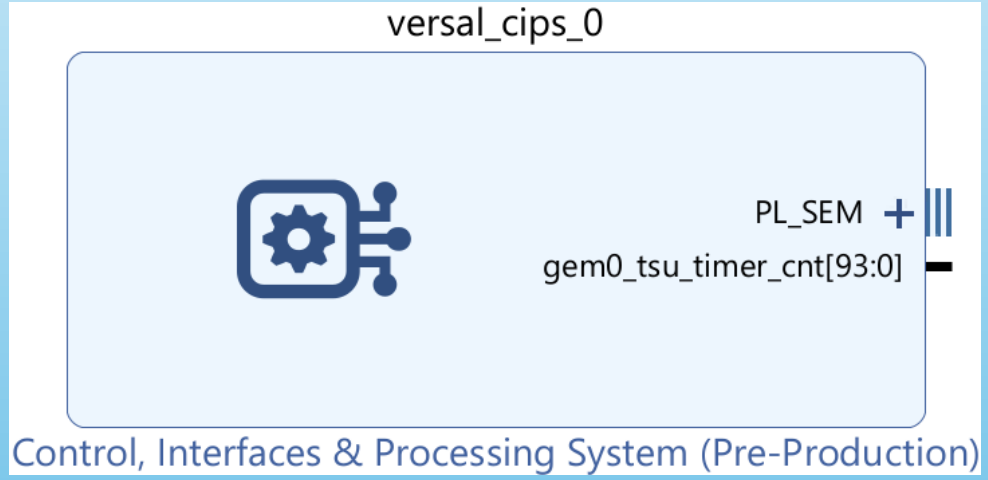
- UC1 (RPU client): R5 in lockstep receives IPI events; logs counts/addresses/status.
- UC2 (Readback): Keep processors idle; periodic bitstream readback for SEU detection.
- UC3 (MicroBlaze client): XilSEM on PMC; MB in PL receives IPI; trade-off: fabric sensitivity.



Lockstep: Safety mode where both RPU cores execute the same instructions in parallel with comparison logic; mismatches flag a fault.

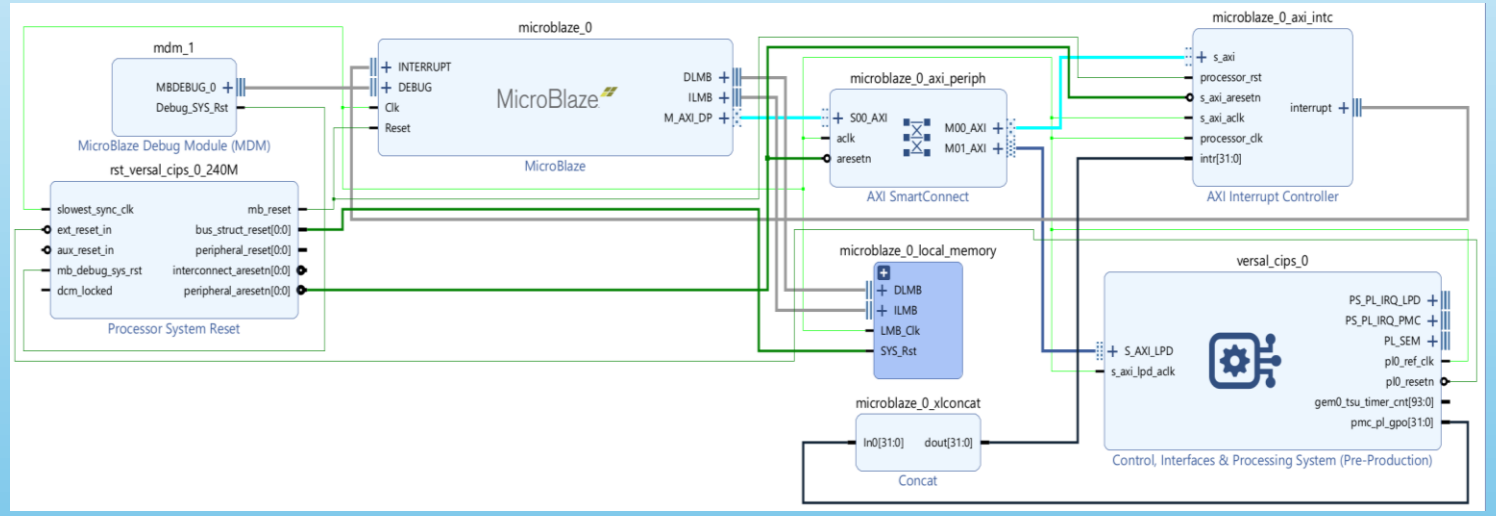
Hardware Setup: RPU Client

- Tools: **Vivado** for hardware; Vitis for software.
- Instantiate CIPS in Vivado: configure PS/PMC, SysMon, XilSEM, PS–PL interfaces, IPI.
- XilSEM: enable deferred start and detect + correct mode.
- Notifications: route IPI 0 → R5-0 so the RPU can receive events.
- Build outputs: Validate, create VHDL wrapper, synthesize/implement, generate bitstream/PDI, and export .xsa to Vitis for the R5 application.



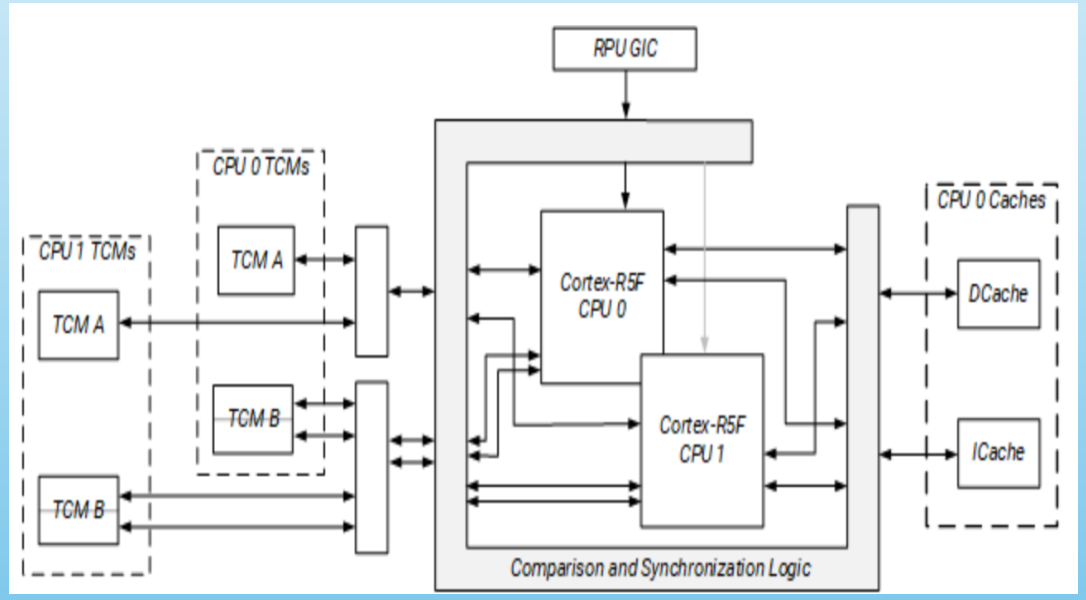
Hardware Setup: MicroBlaze Client

- **Vivado Configuration:**
  - Enable PS→PL interrupt outputs.
  - Route → xlconcat → AXI Interrupt Controller → MicroBlaze IRQ to enable MicroBlaze-XilSEM handshake.
  - Add the debug core (MDM) for JTAG/UART access.
- XilSEM/PLM side
  - XilSEM runs on PMC/PLM; configure it to raise events into the PS_PL_IRQ_* lines when it detects an error.
- This setup can also be used to determine the sensitivity of the MicroBlaze to heavy ion irradiation with XilSEM detecting the upset rate.



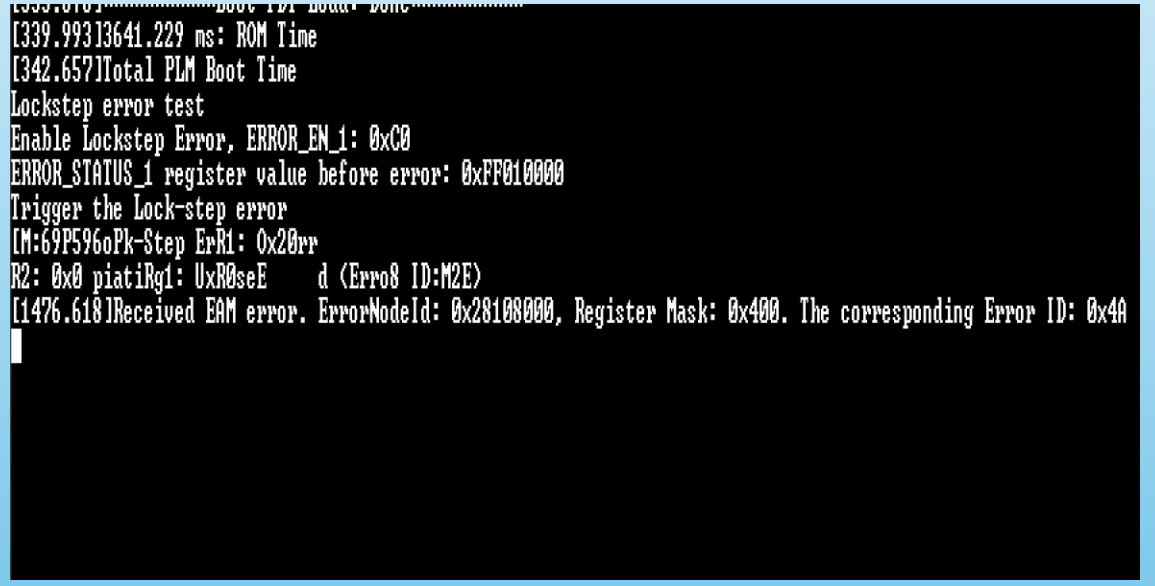
RPU Lockstep Error Injection

- **Objective:** To verify the reliability of the XilSEM-RPU implementation and the operability of the RPU in lockstep mode by:
- Triggering a mismatch in the lockstep registers (RPU_ERR_INJ) of RPU.
- Observing PLM (PMC firmware) initiate the configured recovery (RPU reset) and capturing the UART output.



RPU Lockstep Error Injection (contd)

- For the radiation campaign, and especially for the XilSEM-RPU use case, it can be assured that;
- Under heavy ion irradiation induced upsets, the RPU can reliably operate and when there is a transient fault, the RPU can reset automatically and log the event minimizing the risk of corrupting the error logs.
- The R5 when used as a client to receive IPI notification from XilSEM, is protected by lockstep.



XilSEM CRAM Fault Injection

- Setup: XilSEM-RPU and XilSEM-MB use cases.
- What we inject: Random CRAM bit-flips to emulate radiation — CE, UE, and CRC errors across random frames/qwords (use QWORD 12 for ECC-safe tests).
- What we record: For each error, log the detailed address (frame/FAR, word, qword/bit, row) to verify decode and event delivery.
- Controls & behavior: Select the number of injections; observe RPU lockstep trigger/comparator behavior.

CE = Correctable Error. UE = Uncorrectable Error. CRC = Cyclic Redundancy Error. FAR = Frame Address Register.

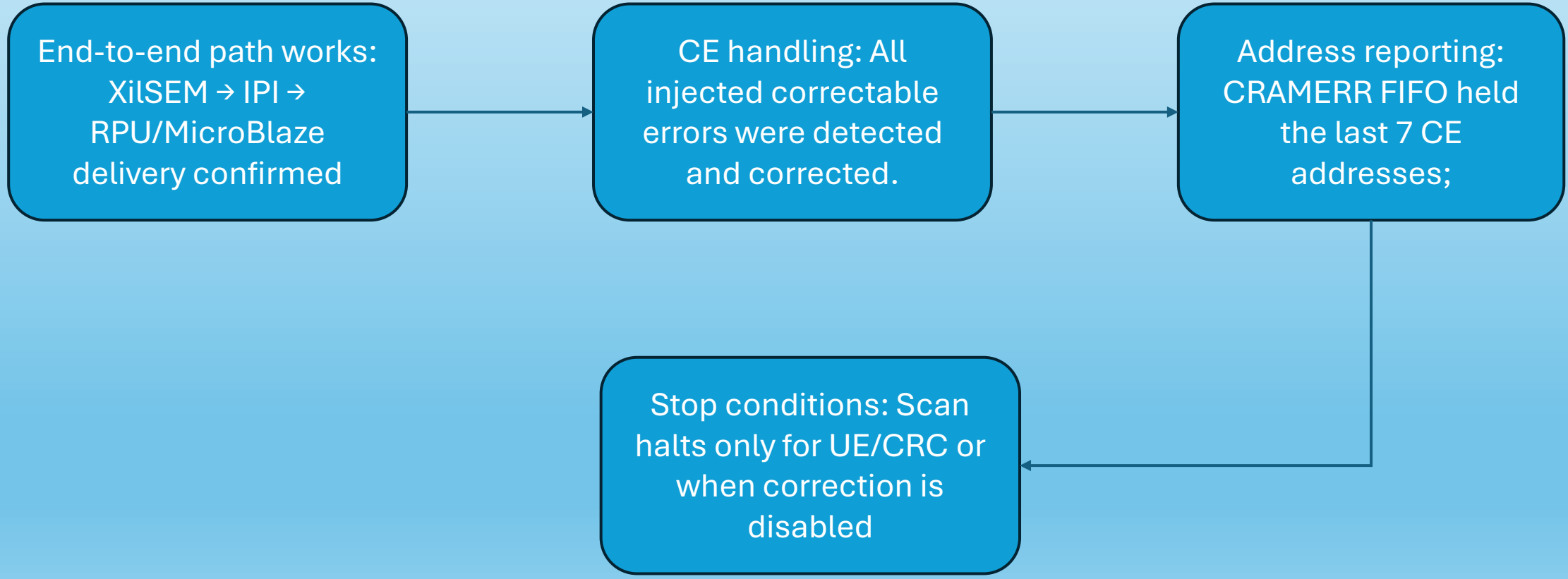
Fault Injection Results (Pre-Beam)

- CEs: detected & corrected; scan continues.
- CRAMERR FIFO: last 7 CE addresses; decoded FAR/qword/bit matched injected address fields.
- UE/CRC: stop/escalate as configured; client/PLM path and logging verified.

```
start_run_112325_201833
Injectig correctable error in [3, 0, 2, 4]... Success
Injectig correctable error in [5, 3, 7, 24]... Success
Injectig correctable error in [0, 12, 6, 5]... Success
Succesfully injected 3 errors
[3, 0, 0]
END
keyword_stop

start_run_112325_201907
Injectig correctable error in [0, 0, 2, 0]... Success
Injectig correctable error in [0, 0, 4, 0]... Success
[0, 1, 0]
ERR
keyword_stop
```

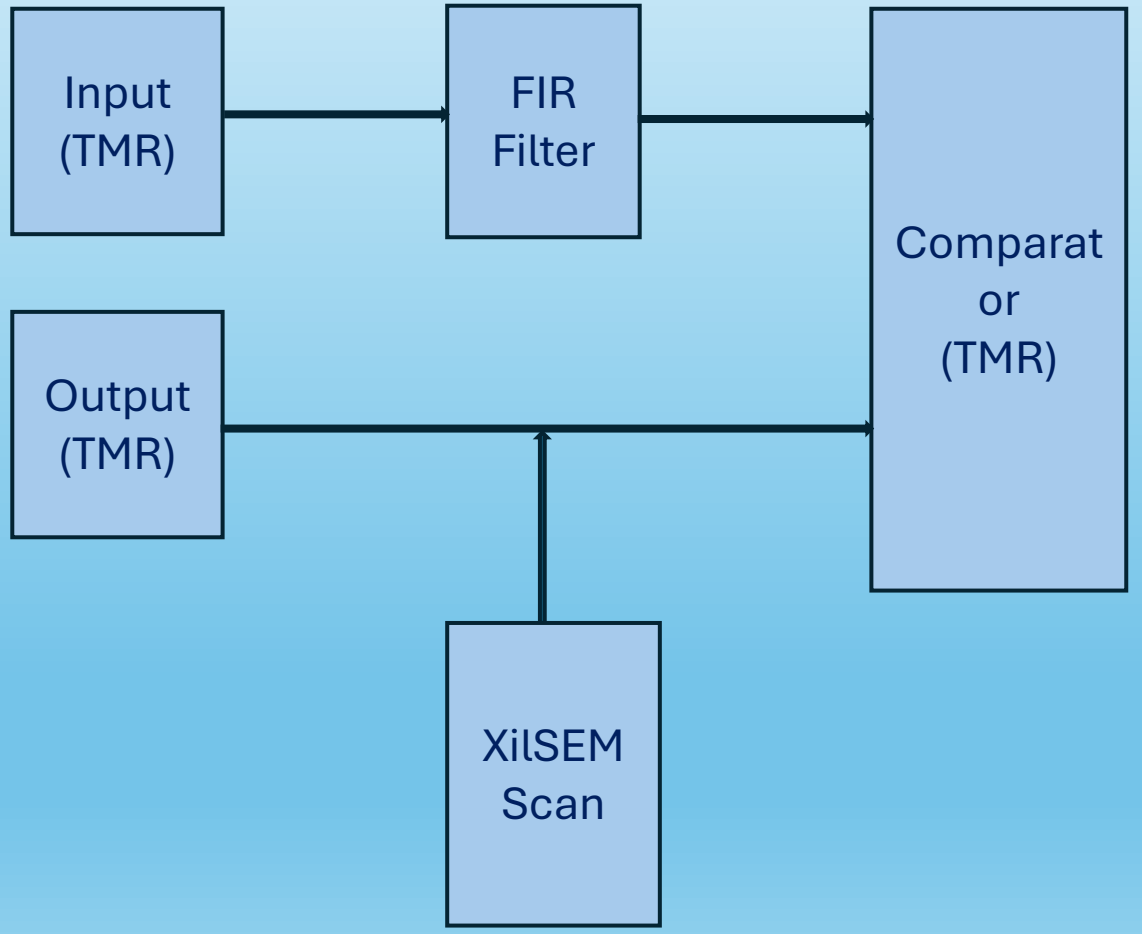
```
start_run_112325_201833
[0, 0, 0]
END
keyword_stop

start_run_112325_201907
[5, 0, 0]
END
keyword_stop

start_run_112425_000123
[13, 4, 0]
ERR
keyword_stop
```

Reliability Implications



DSP Implementation: Design Architecture

- Signal Generation: Implemented as LUTs running at target sample rate
- FIR Filtering: A custom filter, to filter the input signal
- Offset Detection: Comparator monitors the filtered signal and the output, and flags any mismatch/offset
- Error Monitoring: XilSEM scans configuration and reports correctable (CE) and uncorrectable (UE) errors



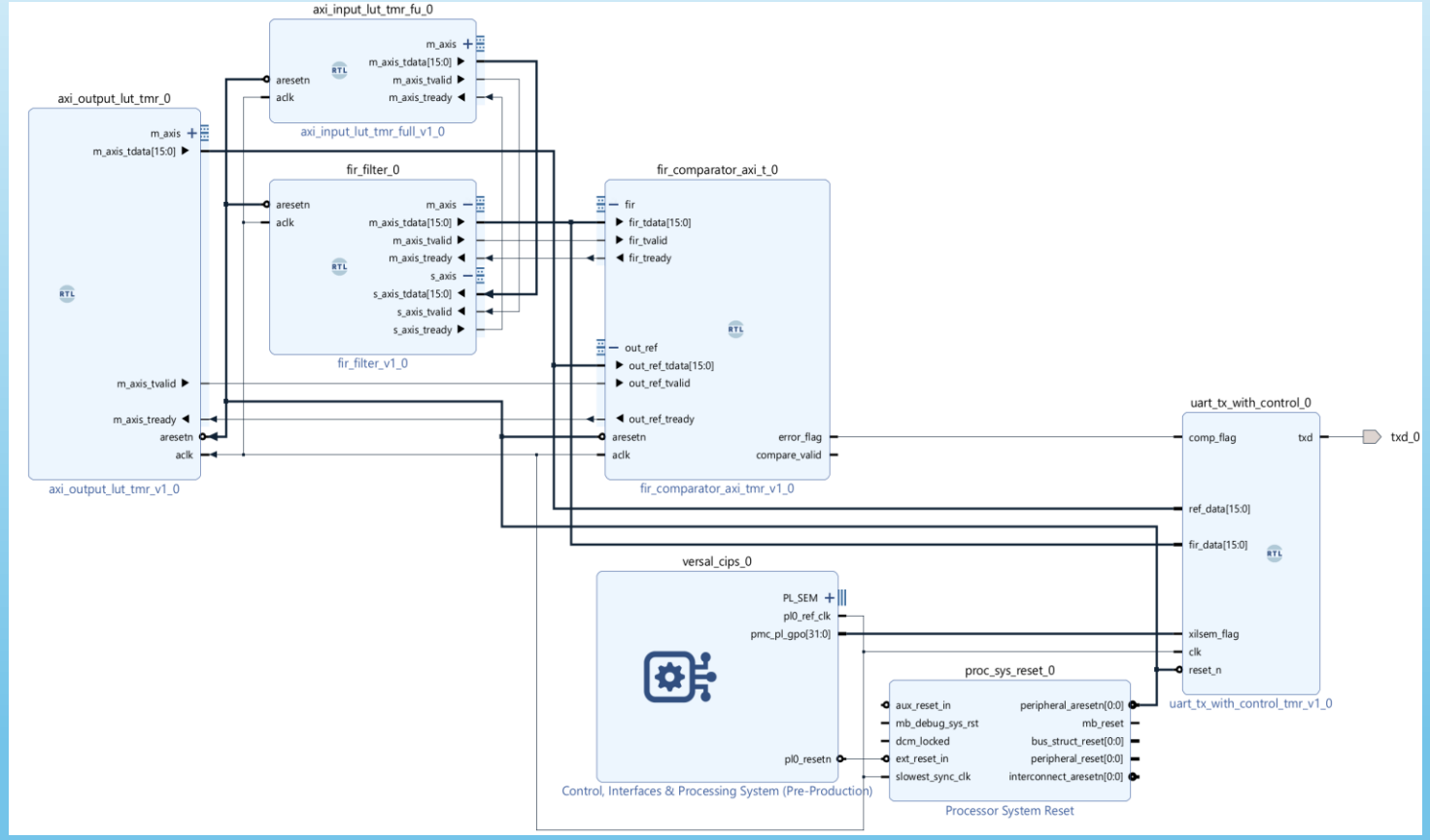
FIR Filter, Input, and Output Specification

- Specified by TASI Electronics Department

Parameter	Specification
Filter Type	Finite Impulse Response (FIR), Low-pass.
Input Signal	Generated via LUT; bandlimited noise + tones to test edge response.
Output	Also generated via LUT; serves as the golden reference. ±0.6 (normalized).
Validation Method	Compare quantized FIR output vs. ideal output.
Observables	Comparator mismtach; XilSEM uncorrectable error count.

Hardware Setup: Vivado Implementation of DSP Design

- axi_input_lut: LUT-based input generator at target sample rate.
- axi_output_lut: LUT-based golden signal generator.
- fir_filter_0: FIR filter mapped to Versal DSP blocks.
- fir_comparator: Comparator + XilSEM for real-time error detection.
- uart_tx_with_control: custom UART module with TX port to PL.



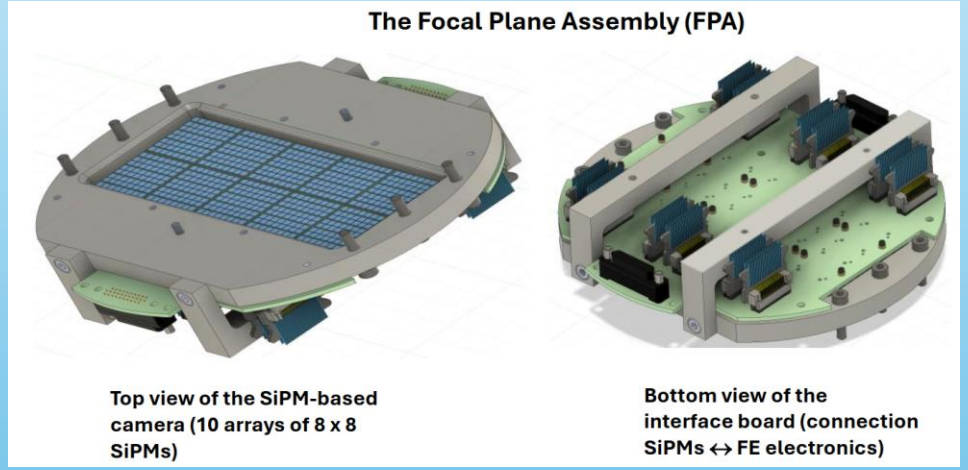
This Vivado block diagram shows the hardware realization of our DSP design

Radiation Beam Characteristics

- Heavy ion: Lead.
- LET available from 12 MeV cm^2 / mg to 33 MeV cm^2 / mg.
- Fluence to be reached per irradiation run between 1E+05 and 1E+06 ions per cm^2.
- Beam is delivered as pulses called “spill”, i.e. beam duty cycle is about 10% with 1s irradiation + 10 seconds stop.
- Beam time request proposal: 12 hour.

Next Steps

- Joined the Terzina Group at UniGE
- Started studying and to perform EQM tests on the Terzina Electronics
- To perform electronics test and validation of the CITIROC readout for Terzina.



Thank you for your attention