ASICs for SiPM Readout
for fast timing and PET applications

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GSSI
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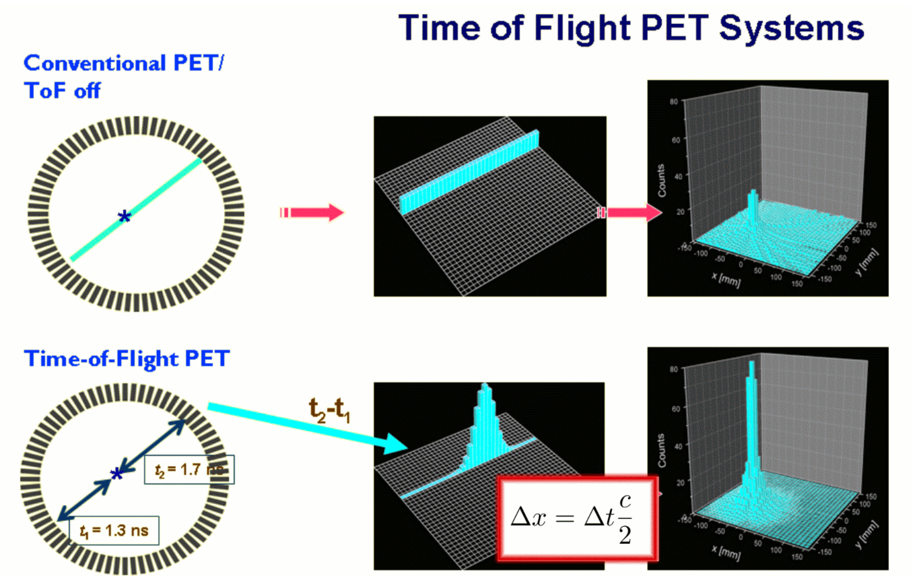

Adapted from: D. Schaart "Prospects for sub-100 picosecond TOF-PET", LPC Clermont-Ferrand, 12-Mar-2014

Why do we need TOF information in PET?

- **TOF for improving equivalent sensitivity**
  - TOF capability $CTR = 200\ ps \Rightarrow \Delta x = 3\ cm$
  - WBS, patient torso $\approx 30\ cm$
  - Gain of 10x in sensitivity[1]
  - More signal, less noise: higher SNR
  - Sharper image, or shorter exam time, or lower tracer dose
- **TOF for background rejection**
- **TOF for direct reconstruction**

[1] counting sensitivity: fraction of emitted *gamma* that are detected

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"Setting the stage" for TOF-capable Electronics

Concept of fast timing requires the definition of the application context:

- ⋆ Timing in the context of TOF-PET refers to Coincidence resolving time, or Coincidence time resolution (CRT, CTR)
  - ↪ precision on resolving the time of arrival of the 2 back-to-back γ-photons

- ⋆ The performance of state-of-the-art PET scanners based on LYSO and SiPMs is currently not limited by the front-end electronics
  - ↪ FEE should preserve the intrinsic performance of the detector
  - ↪ contribution of FEE to SPTR with aSiPMs is

★ **Fast timing**, today, refers to the 10 ps holy-grail

- ⋆ performance (SPTR) of SiPM is quickly approaching this benchmark
- ⋆ a lot is going on the development of new scintillators (e.g. nano-structuring of the crystal surfaces), but...
- ⋆ indeed, the scope of PET imaging is likely to be extended beyond crystals
- ⋆ and, innovative electronics and detectors (other than SiPMs?) are needed

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Front-end Electronics for SiPM readout

- Applications requiring large number of electronic channels and high channel density (e.g PET instrumentation) will require the development of custom integrated electronics

- Typically, all timing systems will call for:
  - ⋆ low-power
  - ⋆ low-noise
  - ⋆ high GBW
  - ⋆ low input impedance

- Different ideas → Different detectors and applications → Different solutions:

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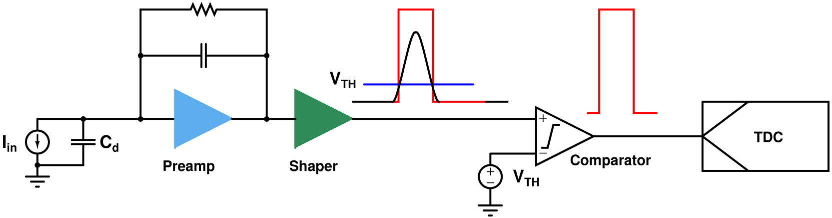
- Different ideas → Different detectors and applications → Different solutions:
  - photosensors (SiPMs, APDs, PMTs, LGADs)
  - crystal one-to-one matching or light sharing with monolithic blocks
  - small-animal, dedicated scanner, full-body scanner
  - DOI reconstruction techniques (crystal patterning, double-side readout)
  - RT or cryogenic operation
  - performance optimisation or cost-driven

Methods for time and energy pick-off with SiPMs

- **Sampling Techniques** (e.g. SAMPIC, DSR)
  - Potentially best time and energy resolution
  - Manageable complexity only for moderate dynamic range
- **Time-based Readout** (e.g. TOFPET, STiC, TRIROC, PETAx)
  - **Constant fraction**
    - Reduces time-walk, potential better time resolution
    - Difficult to implement if signal shape is unknown
    - Difficult to implement for high dynamic range
  - **Single threshold**
    - Easiest circuit topology
    - No hit rejection
    - Excessive jitter for ToT measure? (reduced slope, de-excitation (e.g. L(Y)SO)
  - **Multiple threshold**
    - Easy circuit topology
    - Low-threshold for good timing
    - High-threshold for dark count rejection and ToT measurement
    - Energy measurement can be used for time-walk correction
    - Low jitter requires very fast and low-noise front-end

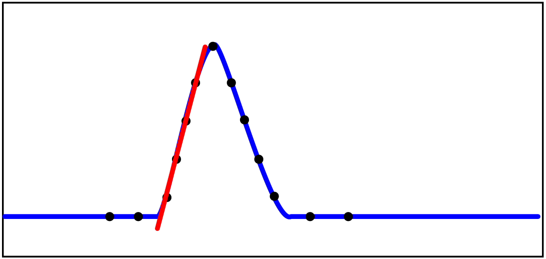
Timing systems: single sample



- The sensor signal is usually amplified and shaped
- A comparator generates a digital pulse
- The threshold crossing time is captured and digitized by a TDC
- TDC can be embedded on the front-end chip or external

▶ Timing is derived from a single sample

Timing systems: multiple samples

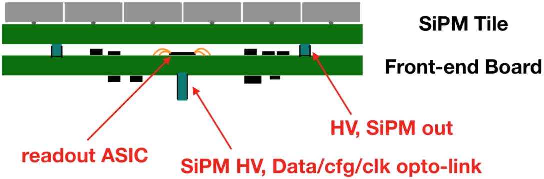


- The sensor signal is usually amplified and shaped
- The full waveform is sampled and digitized at high speed
- In many systems, sampling and digitization are decoupled
- Timing is extracted with DSP algorithms from the digitized waveform samples

▶ Timing is derived from multiple samples

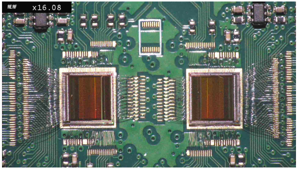
Trends on a-SiPM and readout electronics integration

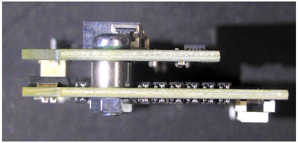
- ⋆ possible sketch of a stack-up SiPM + FEB
- ⋆ Chip-on-board, wire-bonding or flip-chip (FEB hosting ASIC, LDOs, connectors)



- ⋆ ideally, a 4-side abuttable module for large system integration
- ⋆ 2 or 3-tier stack (analogue and digital FEBs)

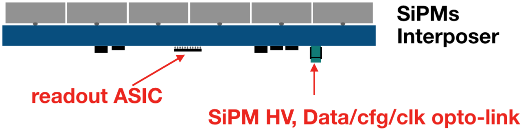
Example of a 128-channel 50 mm^2 integrated electronics front-end module for sensor readout (INFN-TO)





Trends on a-SiPM and readout electronics integration

↪ **Wish list for PET system integrators:**



Likely features of an a-SiPM digital tile for ToF-PET scanners:

- Pixel size O(3x3 mm^2)
- 64 or 128 channels on tile
- power consumption (5 mW)
- fully digital interface
- time and energy measurement

★ Time to Market: **2018-2020**

- early adopters using a-SiPMs and custom ASICs for system integration
- 100 ps target ballpark thoroughly demonstrated on-lab with a-SiPMs
- PET scanner vendors report (from 2017) 200-250 ps CRT system-level performance with SiPMs and LSO
- many (really many) mixed-signal readout ASICs for SiPMs developed since 2010
- Some examples of ready-to-market or commercially available devices:

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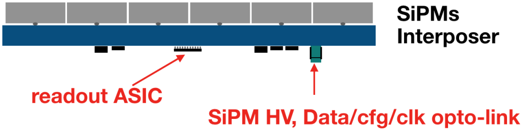

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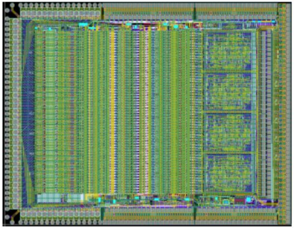
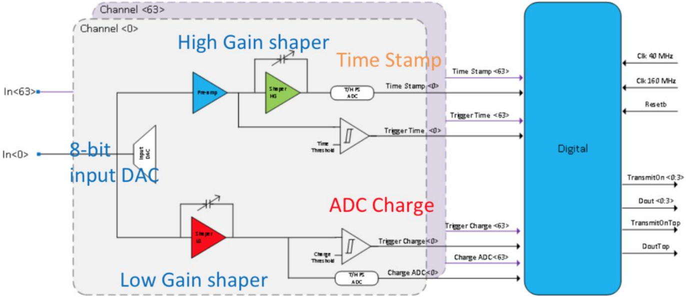
Triroc Description

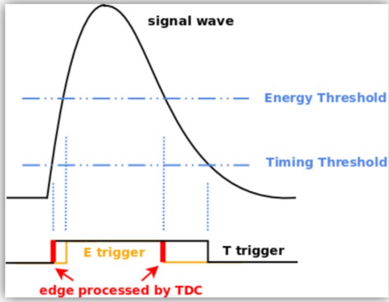
- Full system-on-chip :
  - On-chip zero suppress, self trigger, Time and energy conversion
- 64-channel SiPM readout : positive & negative polarity inputs
- Input DAC for SiPM gain non-uniformity correction
- Time Stamp and ADC charge outputs
- 64-channel trigger outputs
- Power Pulsing : Analog, ADC & Digital
- Event rate : 30k events/s, limited by digital processing

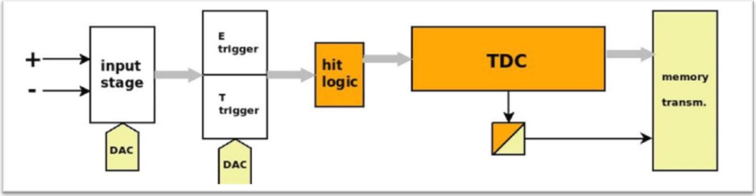




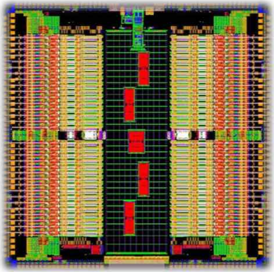
STiC : readout principle

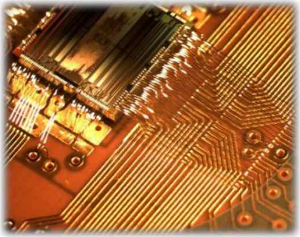
- 64-ch SiPM readout ASIC for Time-of-Flight applications
- UMC 0.18μm CMOS
- Time + (linearized) Energy based on timing measurements
- Analog Frontend + TDC + Digital
- Single-ended (cathode/anode) / differential input
- SiPM bias tuning (~500mV)





STiC – Major specs





TDC bin size	50.2ps@625MHz
TDC DNL	< 0.3 LSB
T threshold range	0.3 – 10 p.e.
E threshold range	> ~4 p.e.
Q inj. Jitter	<20ps
DAC range	> 0.5V
Q resonse	Linear > 2.5pC
power	~25mW/ch
Norminal data rate	40KHz/ch

TOFPET: Design of a readout ASIC for Time of Flight applications

FP7 **EndoTOFPET-US**: combined (Time-of-Flight) PET, ultrasound imaging and endoscopic biopsy

- Need to extract of TOF information to enable endoscopic imaging (enhance SNR)
- FE electronics with very good timing, low-noise, low-power, high density
- TOFPET ASIC developed by LIP in the framework of FP7/EndoTOFPET-US project

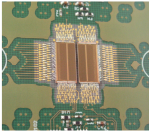
Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate

ENDO TOFPET US
Endoscopic TOFPET & Ultrasound

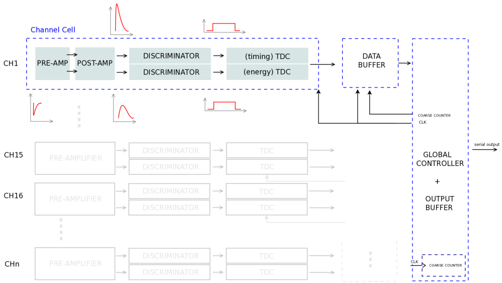
The 64-channel TOFPET chip in a nutshell:

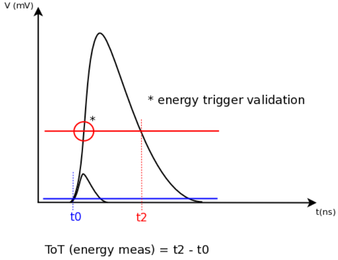
- amplification, signal condit. and time-to-digital conversion
- 25 ps r.m.s. intrinsic resolution
- fully digital output, data rate up to 640 Mb/s
- optimized for low-power (less than 10 mW p/channel) and high-rate (160 kHz/channel)



M D Rolo et al, **TOFPET ASIC for PET applications**, 2013 JINST 8 C02050
M D Rolo et al, **A low-noise CMOS front-end for TOF-PET**, 2011 JINST 6 P09003

TOFPET: Overview of the channel architecture

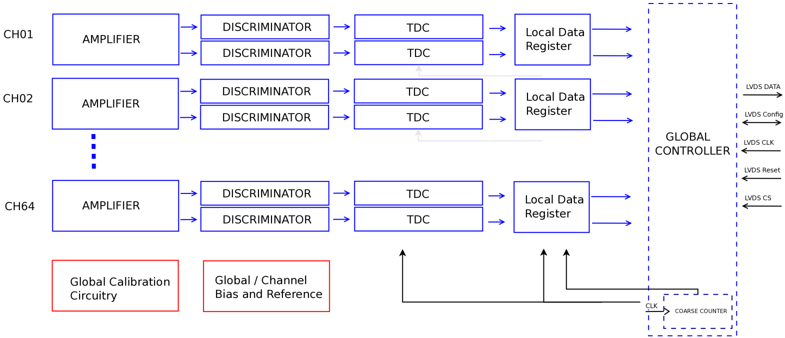




- gm-boosted common-gate input stage, allows SiPM HV bias adjustment - Positive or negative signal polarity
- Charge measured with Time-over-threshold
- Time and charge measurements with independent TDCs
  - t0: 50 ps time stamp from rising edge of DOT
  - t2: 50 ps time stamp from falling edge of DOE
- Trigger level **0.5 p.e.** with SNR = 25 dB
- Low-power 8-11 mW p/channel

TOFPET: Overview of the chip architecture

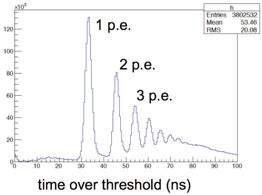
The TOFPET ASIC is a 64-channel analogue mixed-signal chip, output is fully digital. The periphery of the chip hosts the calibration and bias circuitry.

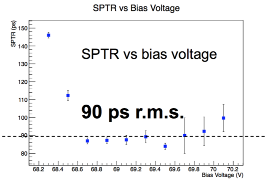


- LVDS 10 MHz SPI configuration link and dark count measure
- 2x LVDS up to 640 Mbps data output interface; 8B/10B encoding
- On-chip DACs and reference generators

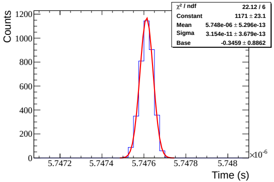
TOFPET: characterization results

- Single-photon time resolution (420nm light pulser)

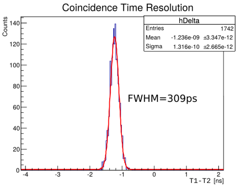




- MPTR: 32 ps sigma (intrinsic time resolution of channel)



- CTR: 310 ps FWHM
  - Two LYSO 4x4 crystal matrices: crystal size 3.5 x 3.5 x 15 mm^3
  - 16-channel MPPC 3x3 mm^2 matrix

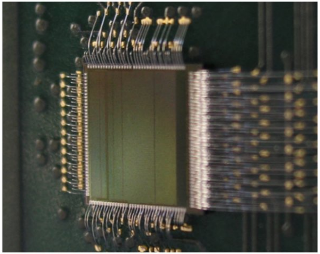


PETsys
Electronics

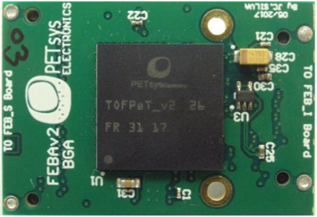
PETsys TOFPET2 ASIC

From analog frontend to digital system interface

- 64 independent channels in 5x5 mm^2
- Standard CMOS 110 nm
- Positive or negative signal polarity
- Dynamic range 100 fC - 1500 pC
- Noise 1.5 mV (1 p.e. ~ 30 mV)
- Charge integration ADC 10 bit
- TDC time binning 30 ps
- Low power: <12.5 mW/Ch
- Very high event rate capability up to 30 Mcps per ASIC *)
- On-chip calibration circuitry



TOFPET2 chip-on-board



PETsys Electronics

CTR with different SiPMs

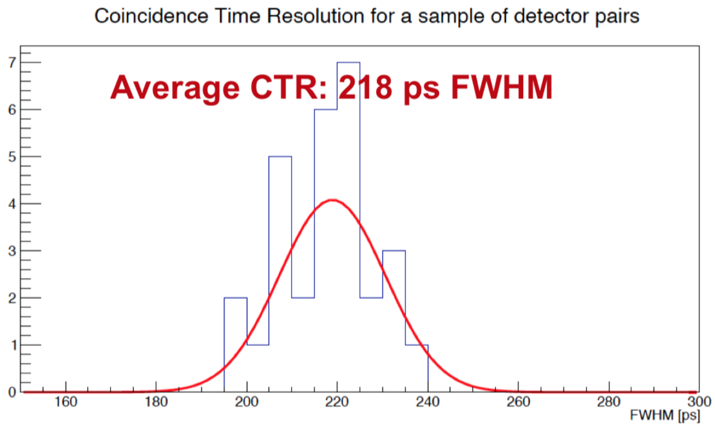
- CTR measurements were performed with **individual LYSO crystals of 3x3x5 mm^3** glued to **SiPMs 3x3mm^2 of several producers**
- **One-to-one crystal-SiPM coupling with the same area**
- The uncertainty of these measurements is estimated at 15 ps. The observed differences between the three SiPMs are not statistically significant.

SiPM type	SiPM area (mm2)	Over-voltage (V)	CTR FWHM (ps)
KETEK-PM3325-WB	3x3	4	229
HPK MPPC S13361-3050AE-04	3x3	5.5	215
SensL ArrayJ-30035-64P-PCB	3x3	5	228

CTR with LYSO array of 4x4x15mm AC coupling; T=18 ºC

PETsys Electronics

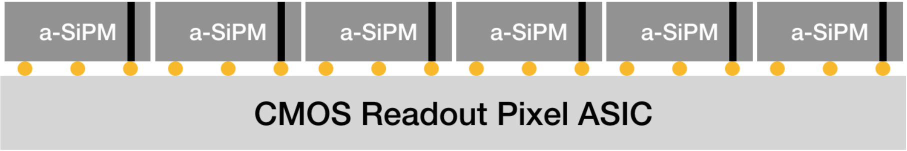
Broadcom array AFBR-S4N44P163; 30 µm cells
OV= 8.5 V
T=18 ºC

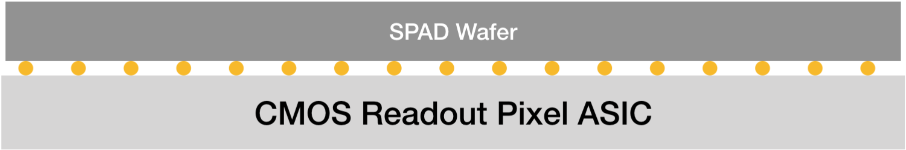


Performance summary

- Remarkable set of measurements with TOFPET2, a 64-channel ASIC for SiPM readout and digitization in TOF applications:
  - Amplifier noise σ ~ 0.1 p.e. rms
  - TDC DNL<0.1 LSB; INL<1 LSB
  - Time resolution: 26 ps r.m.s
  - SPTR = 90 ps r.m.s (w/ HPK S31361-3050 @ 7.5 V over-voltage)
  - CTR = 127 ps FWHM (w/ LYSO 2x2x3 mm3 ;NUV-SiPM 4x4 mm FBK / Broadcom)
  - ADC DNL <0.5 LSB; INL<1 LSB
  - Charge integration noise: 0.65 LSB r.m.s.
  - Energy resolution 511 keV = 10.5% (w/ LYSO; SiPM KETEK PM3325)

What's Next?





- ★ Hybrid CMOS and aSiPM matrix (mm-range pixel), or
- ★ 3D-SiPM matrix mounted on top of a CMOS wafer
- ★ Back-side illuminated or Front-side illuminated with TSVs

Next generation 3D digital SiPM for precise timing resolution

Jean-François Pratte

F Nolet, W. Lemaire, F. Dubois, N. Roy,
S. G. Carrier, A. Samson,
G. St-Hilaire, S. A. Charlebois, R. Fontaine

Interdisciplinary Institute for Technological Innovation (3IT),
Université de Sherbrooke

14th Frontier Detectors for Frontier Physics 2018

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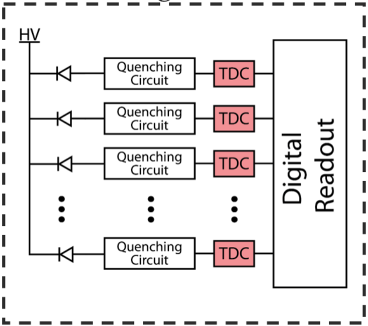
GRAMS

Benefits of Digital SiPM for TOF-PET

Advantages
- 1 TDC per SPAD
- Uniform SPTR per pixel
- SPAD to SPAD skew correction

Cons of 2D implementation
- Low fill factor
- Same process for SPAD and CMOS
- No room for digital signal processing

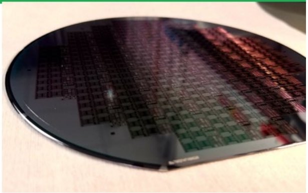
2D Digital SiPM



Digital SiPM

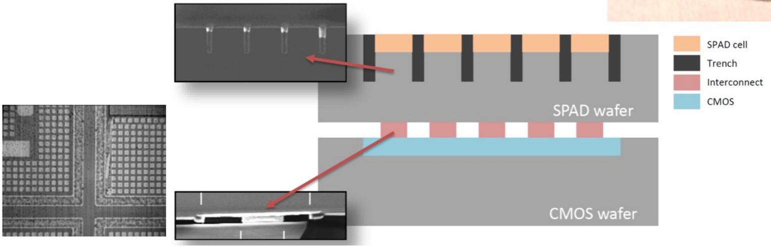
3D d-SiPMs

Next Generation 3D Digital SiPM with CMOS 65 nm readout



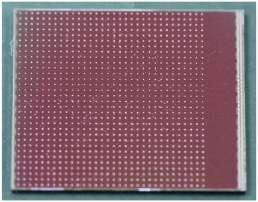
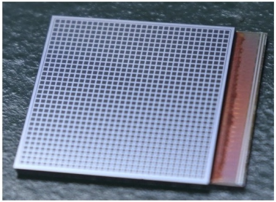
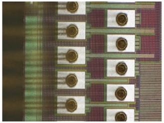
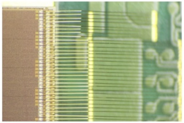
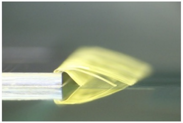
3D Integration

- High fill factor
- Heterogeneous technologies integration:
  - SPAD array: Teledyne-Dalsa custom process
  - **TSMC CMOS 65 nm - 256 SPAD readout ASIC**



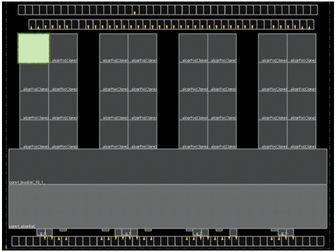
3D a-SiPMs?

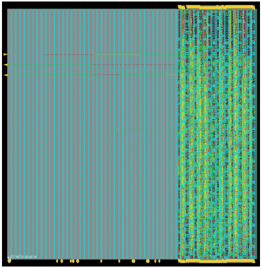
- CMOS 1024-pixel readout ASIC for fast timing applications developed by INFN-TO
- UMC 110nm technology
- Pixel size 400 μm, 32x32 pixel matrix, approx 250 mm^2

- flip-chip mounted to a photosensor (*top right*). Detail of bonding pads (*bottom*) and bonding scheme for data and power
- The first-silicon ASIC performs single-photon time-tagging with a 30 ps r.m.s. time resolution, up to 200 kHz per pixel

ALCOR - A Low Power Chip for Optical Sensor Readout





- Development in the framework of the **Darkside Collaboration**, targets operation at 87K
- 32-pixel matrix mixed signal ASIC
- amplification, signal conditioning and event digitisation, and features fully digital I/O.
- each pixel reads an SiPM (up to 1 cm^2, compatible with smaller pixels)
- Pixel hosts SiPM VFE, LET discriminator, 4 TDCs, control and interface
- Single-photon time tagging mode <u>or</u> time and charge measurement
- 64-bit (32-bit on time tagging mode) event data generated on-pixel
- Up to 4 LVDS TX data links used, SPI for chip configuration
- operation from 10 MHz up to 320 MHz (TDC binning down to 50 ps)
- Towards 3D hybrid integration

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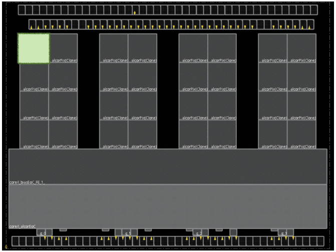

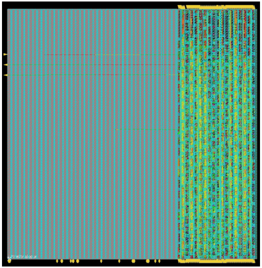

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Outlook for SiPM readout on a Million-Channel LAr PET Scanner

- Room Temperature mixed-signal ASICs for SiPM readout available for system-level integration on Time-of-Flight PET instruments
- LYSO-SiPM based PET scanners' performance limited by scintillation statistics
- LAr and LXe could become core technologies towards the 10's ps range ?
- Research on Dark Matter and Neutrino Experiments could produce innovative integrated electronics for fast timing in cryogenic temperature
- **INFN promoting and developing** cryogenic integrated circuits for Darkside-20K
- INFN Collaboration with Sherbrook University on the study of silicon interposer technology
- INFN Collaboration with PSI, BNL, Fermilab, Sherbrook on CMOS modelling for cryogenic operation
- Ramp-up of INFN-LFoundry technical assessment for advanced sensor integration and development of large active silicon interposers for cryogenic applications