Terzina Meeting
Nov 23rd, 2022 - Turin, Italy

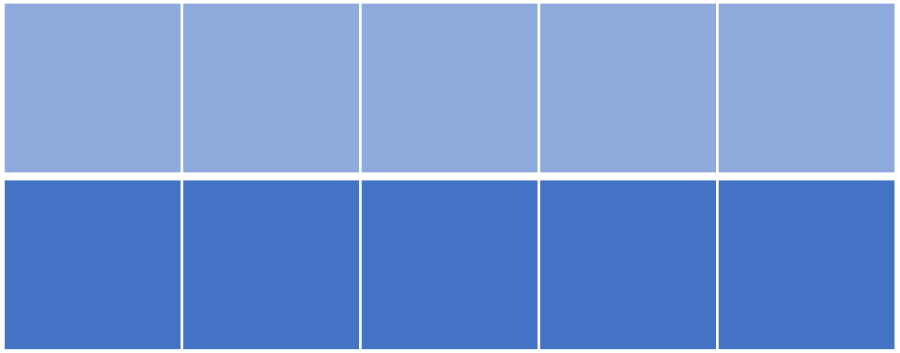
FPGA Updates

GRAN SASSO SCIENCE INSTITUTE

Istituto Nazionale di Fisica Nucleare

GIAMPAOLO Raffaele Aaron

General Info

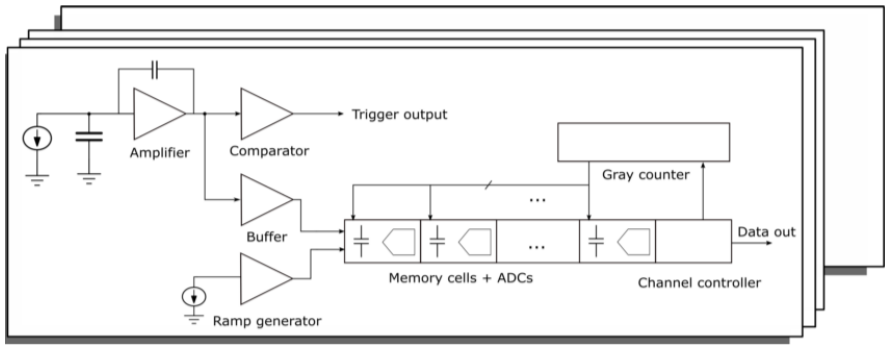


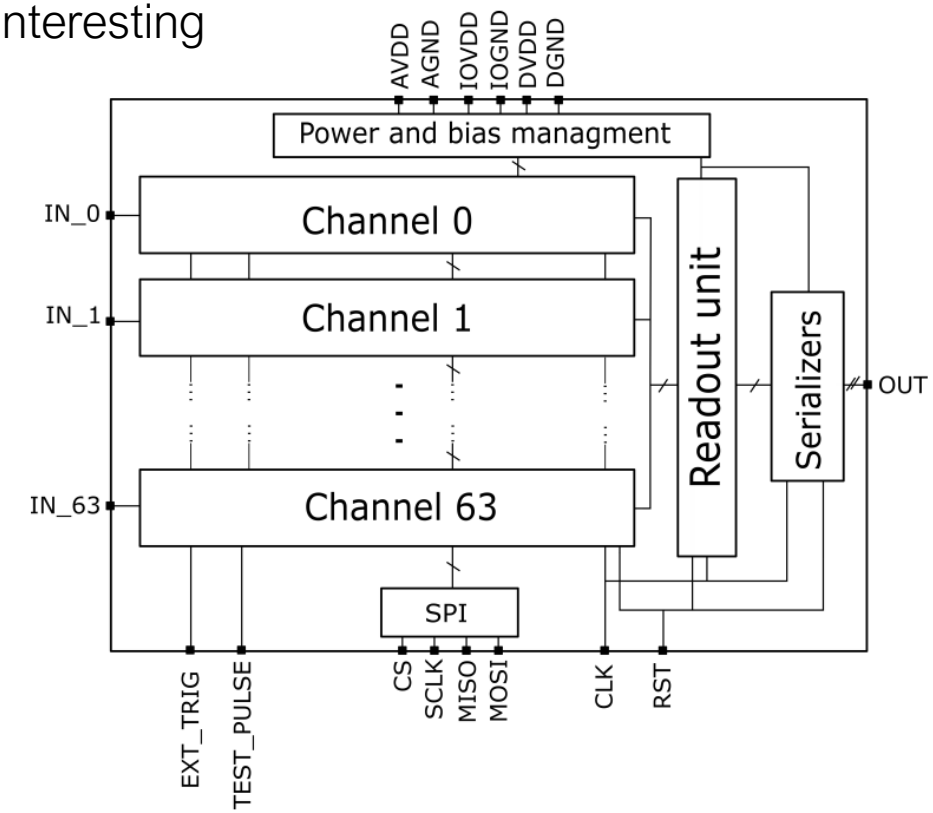
General info:

- 10 SiPM modules
- Each module includes 8 × 8 SiPM
- 1 ASIC per SiPM module
- 5 bottom modules have interesting

ASIC info:

- One ASIC reads one SiPM module
- Each ASIC has up to 8 differential outputs (16 out pads)
- 65nm CMOS technology and will include 64 channels
- 256 memory cells per each channel
- 12b Wilkinson ADC per each channel



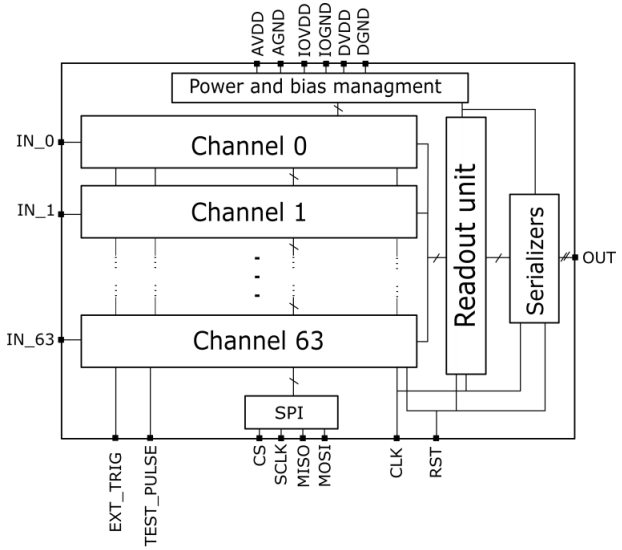


ASIC I/O Info

PIN name	PIN type	Purpose	Description	Required PADs Per ASIC	Required PADs Per FPGA	
RST	analog I/O	digital input	Reset signal	2	2	
CLK	analog I/O	digital input	Clock signal	2	2	
SER OUT	analog I/O	digital output	Output of the serializer	16	160	Could be 90
EXT TRIGGER	analog I/O	digital input	External trigger	2	2	
TEST PULSE	analog I/O	digital input	Control signal to test the analog channels		0	
CS	analog I/O	digital input	Chip select for the SPI interface	4	4	→ TBD
MOSI	analog I/O	digital input	Master Output Slave input from the SPI interface	2	2	→ TBD
MISO	analog I/O	digital output	Master input Slave Output to the SPI interface	2	2	→ TBD
			total	30	174	

FPGA & ASIC info:

- Serializer CLK = 400 MHz DDR
- Storage IP either BRAM or external RAM
- Need radiation tolerant FPGA (500 rad/y)

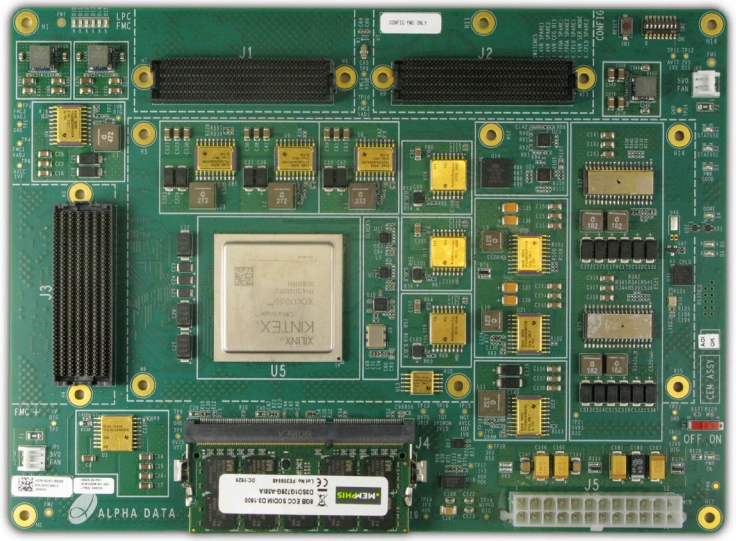


FPGA Choice Info

FPGA possibilities:

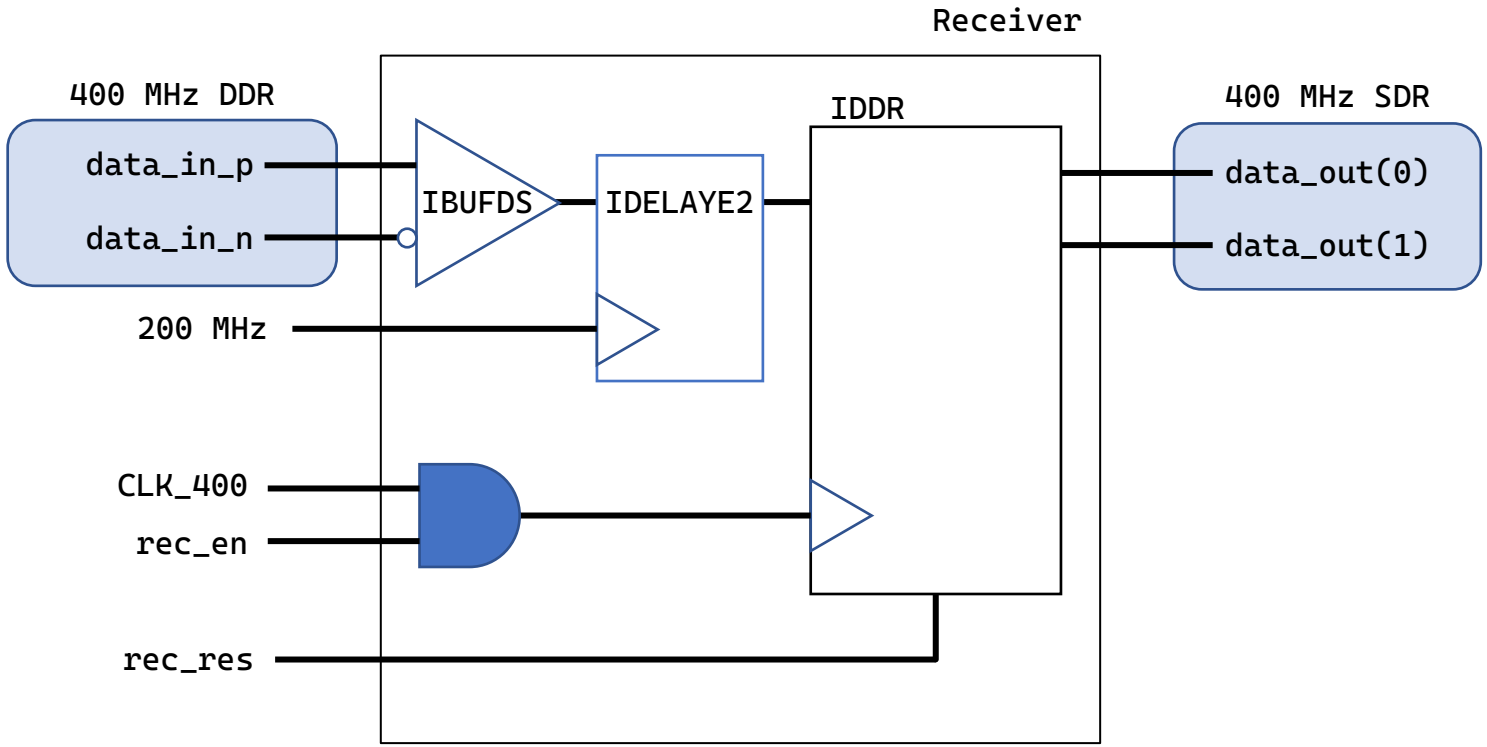
- Genesys 2 Kintex-7 FPGA Development Board (LINK)
- Cost < 2 k€
- Commercial FPGA
- More IOs

- ADA-SDEV-KIT3 Xilinx XQRKU060 (LINK)
- Cost > 20 k€
- Space Grade components
- Radiation tolerant process and layout
- IOs are scarce, but enough



Receiver

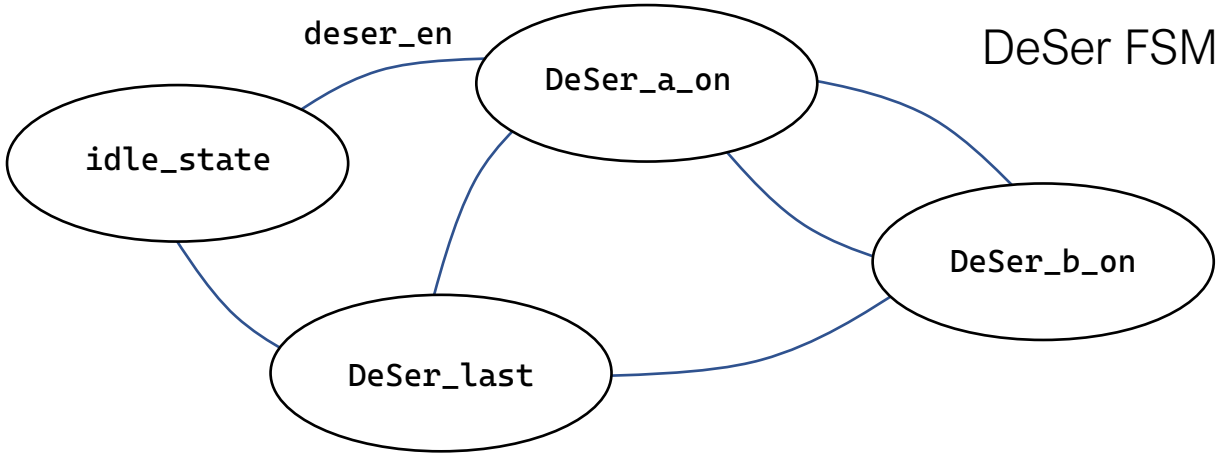
```
entity receiver is
    generic(
           N : integer := 2
    );
    Port ( data_in_n    : in  STD_LOGIC;
           data_in_p    : in  STD_LOGIC;
           CLK_400      : in  STD_LOGIC;
           rec_res      : in  STD_LOGIC;
           rec_en       : in  STD_LOGIC;
           data_out     : out STD_LOGIC_VECTOR (N-1 downto 0));
end receiver;
```

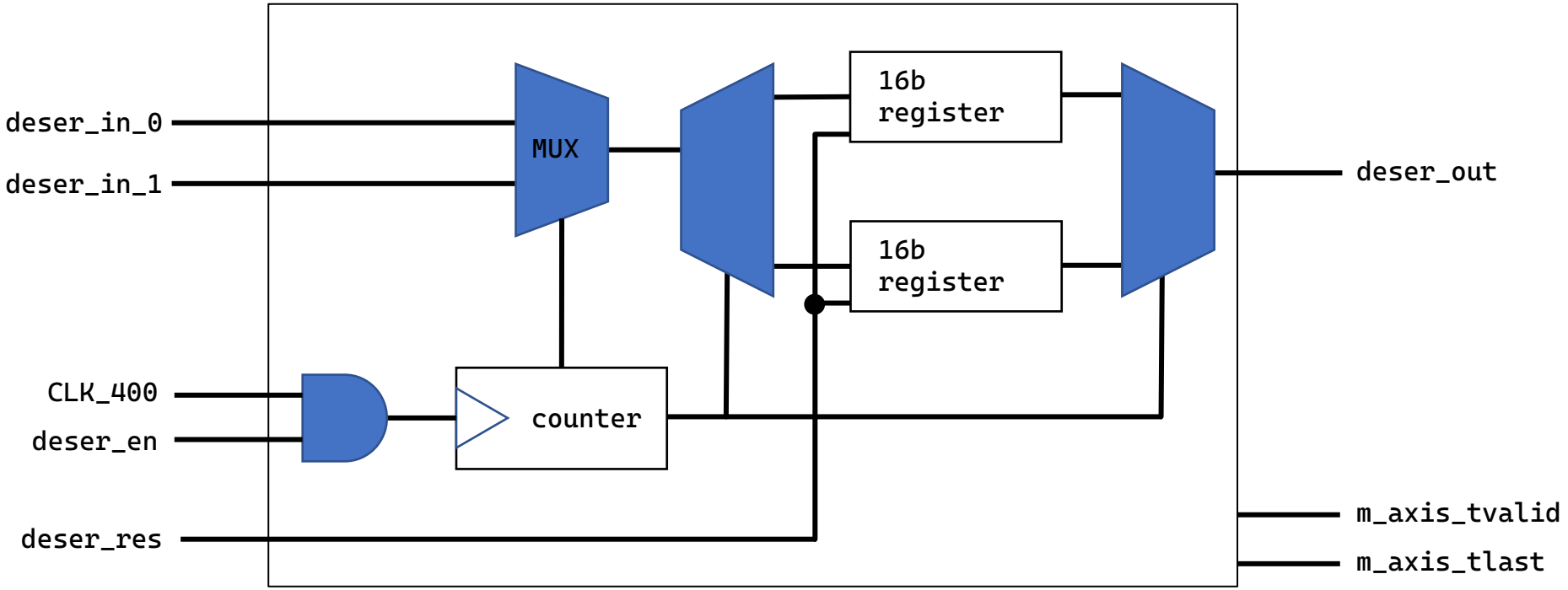


data_out(0) changes with the rising edge of CLK_400
data_out(1) changes with the falling edge of CLK_400

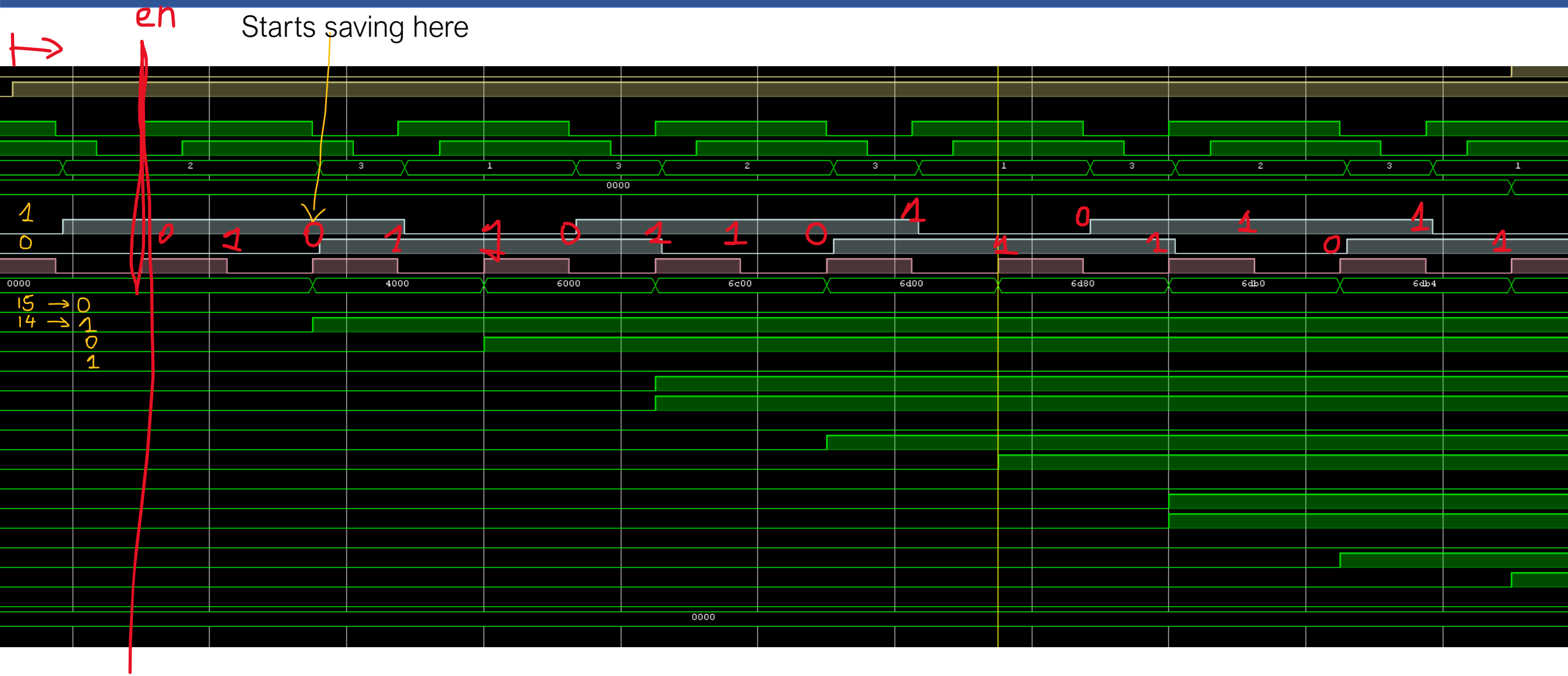
```
entity DeSer is
  Port ( clk              :   in  STD_LOGIC;
         deser_res        :   in  STD_LOGIC;
         deser_in_0       :   in  STD_LOGIC
         deser_in_1       :   in  STD_LOGIC;
         deser_en         :   in  STD_LOGIC;
         m_axis_tlast     :   out STD_LOGIC;
         deser_out        :   out STD_LOGIC_VECTOR (16b)
         m_axis_tvalid    :   out STD_LOGIC := '0'
         );
end DeSer;
```

DeSer FSM



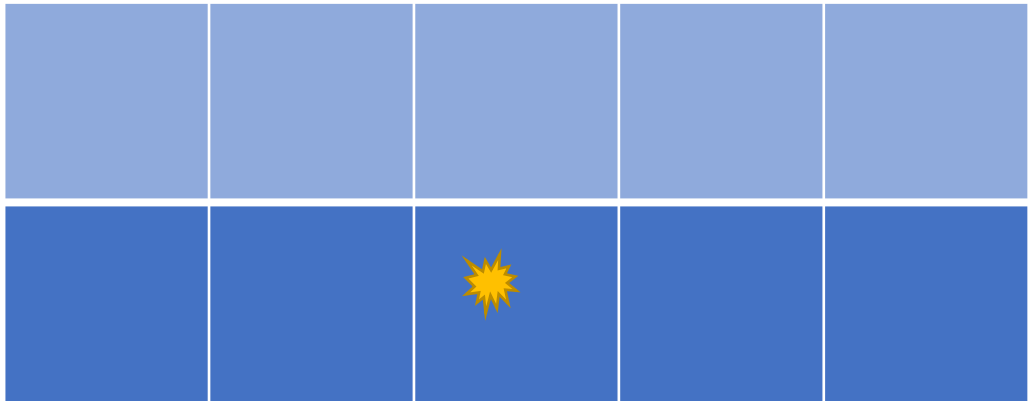


DeSer Simulation

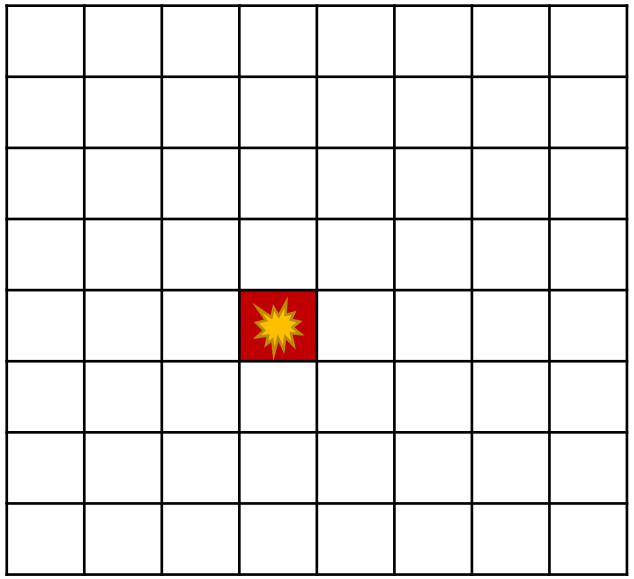


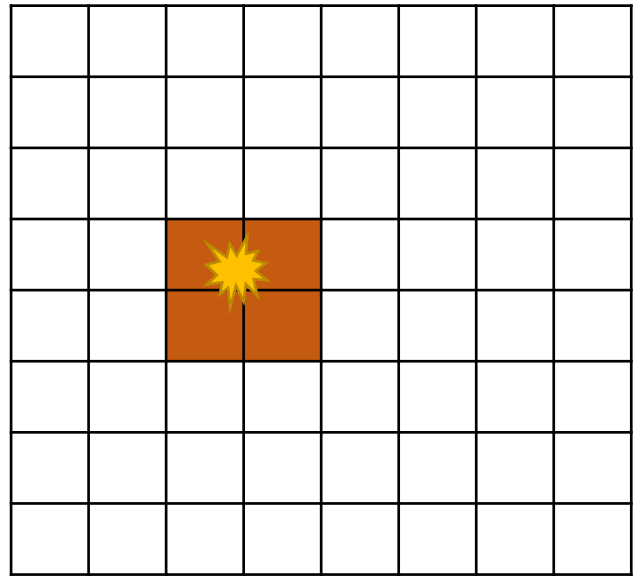
2-threshold trigger

```
component HitValidator
     Port ( a     : in  STD_LOGIC_VECTOR (63 downto 0);
            clk   : in  STD_LOGIC;
            valid : out STD_LOGIC;
            done  : out STD_LOGIC;
            start : in  STD_LOGIC);
 end component;
```



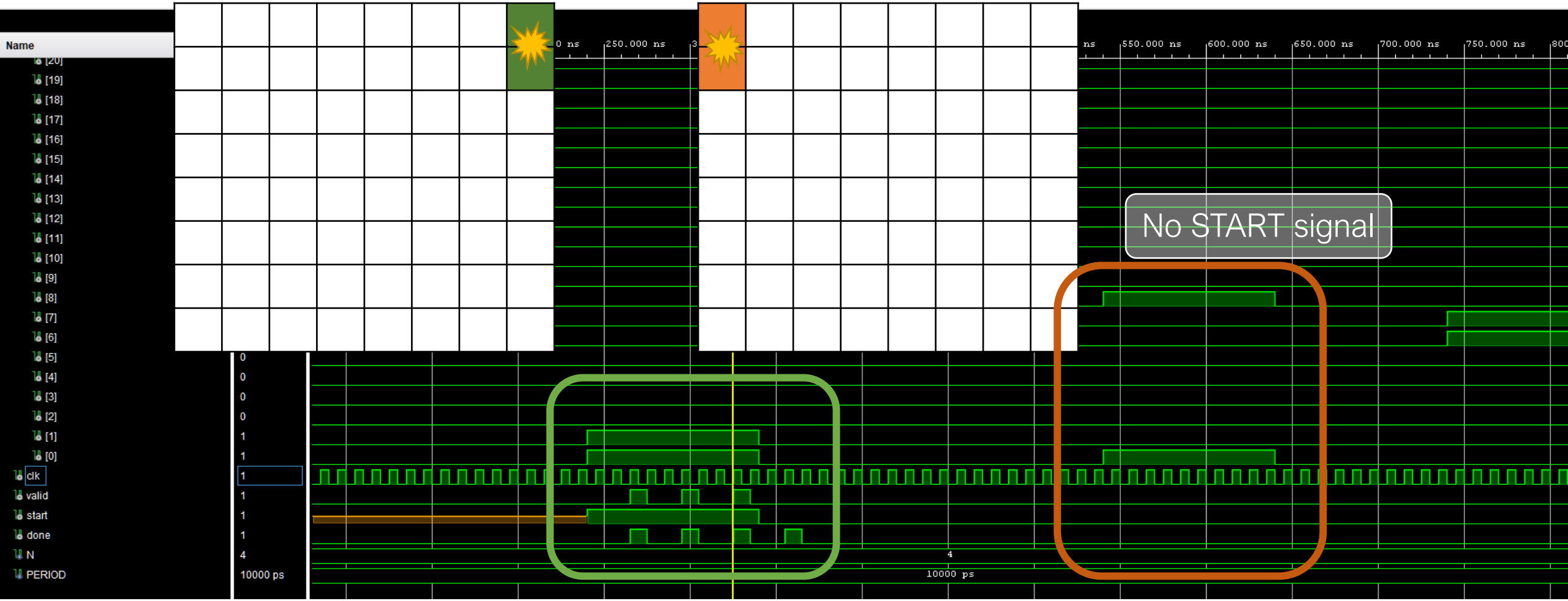
2-threshold trigger:





- If the highest threshold is crossed send out the data;
- If more than x (e.g., 2 < x < 9) low thresholds are crossed send out the $V_{th,min}$ hitmap;
- If contiguous pixels extract data.

Hitmap validator simulation



Power

The power dissipation must be accounted for, it seems to be higher than our budget of 4 W.

On the right the static and dynamic dissipation values of an **ARTY Evaluation board**, running the validation VHDL, with **64 inputs and 2 outputs** are shown.

Here the CLK and START signals are not indicative as they are sent from an outside source. (They are input pins here)

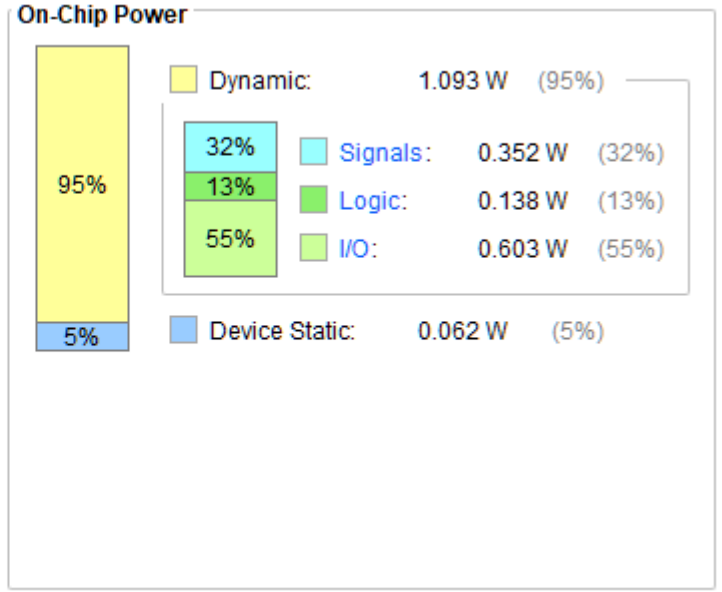
The dissipated power figures lead to an estimation of **more than 4 W** only for the FPGA.

- ~ 2 W for 10 Outputs pins
- ~ 1 W for 160 input pins
- > 500 mW for processing and static power

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.155 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.5°C**
Thermal Margin:	69.5°C (14.5 W)
Effective ϑJA:	4.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



I/O

Utilization	Name	I/O Type	I/O Standard	Drive Strength	Input Pins	Output Pins
0.603 W (52% of total)	HitValidator					
0.243 W (21% of total)	a	HR	LVCMOS18	N/A	64	0
0.219 W (19% of total)	valid	HR	LVCMOS18	12.000	0	1
0.134 W (12% of total)	done	HR	LVCMOS18	12.000	0	1
0.004 W (1% of total)	clk	HR	LVCMOS18	N/A	1	0
0.004 W (1% of total)	start	HR	LVCMOS18	N/A	1	0

Conclusions

- Focused on Genesys 2 as possible first FPGA testbench
- Hitmap validator code has been written and tested
- Receiver designed, but needs upgrade for higher speed (ISERDESE2 implementation)
- Power is out of specs: we require a higher power budget if we want to continue with the provided specifications

Possible solution: proximity FPGA & higher power budget

Thank you,

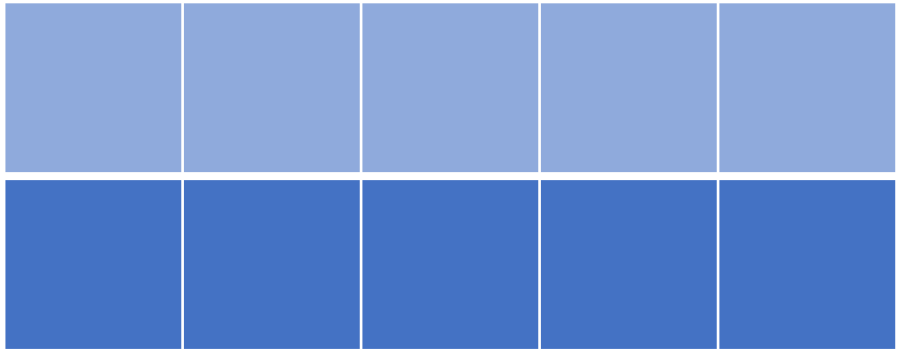
Raffaele Aaron Giampaolo

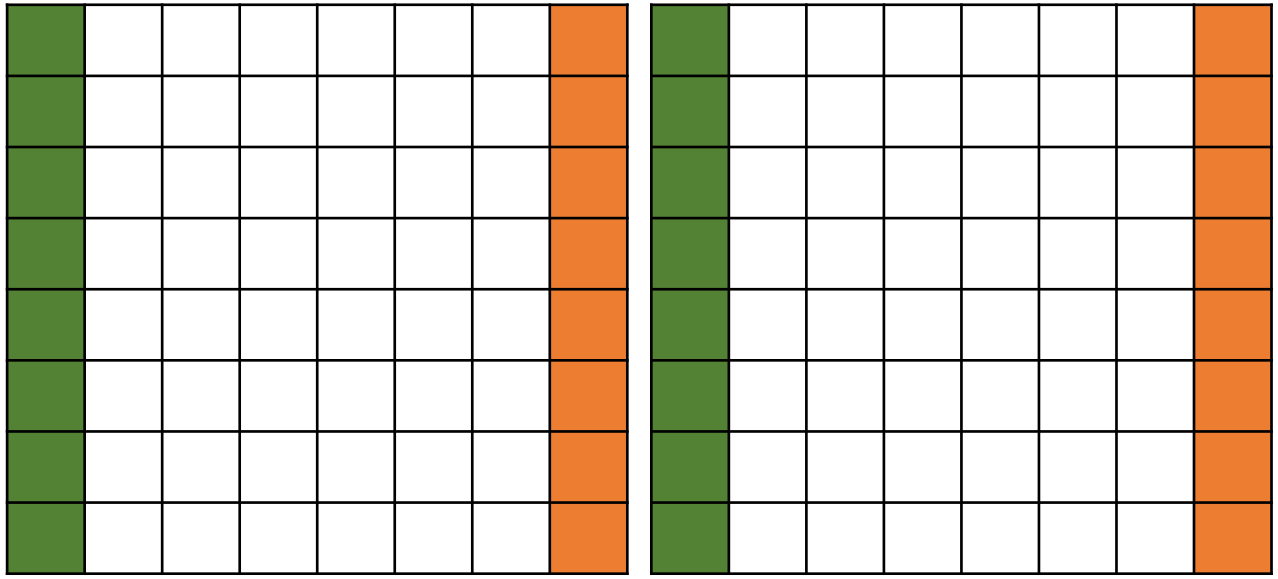
GRAN SASSO
SCIENCE INSTITUTE

Istituto Nazionale di Fisica Nucleare

BACKUP

Readout methods





Full camera:

- 10 8×8 SiPM (3 × 3 mm²) modules;
- Bottom modules facing limb (interesting);
- Top modules facing ground, less interesting (for now)

More ideas:

- connect the bottom modules with all the 8 serializers enabled, while keeping the top modules read out only by a single serializer;
- Use 3 serializers for the bottom modules which would tell the FPGA that border signals have been acquired (needs to be implemented on ASIC, time consuming) (less power & interconnections)